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Accurate ZVS Analysis of a Full-Bridge T-Type Resonant Converter for a 20-kW Unfolding-Based AC-DC Topology

Shubhangi Gurudiwan, ***Graduate Student Member, IEEE***, **Aditya Zade**, ***Graduate Student Member, IEEE***, **Hongjie Wang**, ***Senior Member, IEEE***, and **Regan Zane**, ***Senior Member, IEEE***

Department of Electrical and Computer Engineering, Utah State University, Logan, UT 84341 USA

CORRESPONDING AUTHOR: Shubhangi Gurudiwan (e-mail: shubhangi.gurudiwan@usu.edu).

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ABSTRACT Unfolding-based single-stage ac-dc converters offer benefits in terms of efficiency and power density due to the low-frequency operation of the Unfolder, resulting in negligible switching losses. However, the operation of the Unfolder results in time-varying dc voltages at the input of the subsequent dc-dc converter, complicating its soft-switching analysis. The complication is further enhanced due to the nonlinear nature of the output capacitance (C_{oss}) of MOSFETs employed in the dc-dc converter. Furthermore, unlike two-stage topologies with a constant dc-link voltage, as seen in high-frequency grid-tied converters, grid voltage fluctuations also impact the dc input voltages of the dc-dc converter in unfolding-based systems. This work comprehensively analyzes the soft-switching phenomenon in the T-type primary bridge-based dc-dc converter used in unfolding-based topologies, considering all the aforementioned challenges. An energy-based methodology is proposed to determine the minimum zero-voltage switching (ZVS) current and ZVS time during various switching transitions of the T-type bridge. It is shown that the existing literature on the ZVS analysis of the T-type bridge-based resonant dc-dc converter, relying solely on capacitive energy considerations, substantially underestimates the required ZVS current values, with errors reaching up to 50%. The proposed analysis is verified through both simulation and hardware testing. The hardware testing is conducted on a 20-kW 3-ϕ unfolding-based ac-dc converter designed for high-power electric vehicle battery charging applications. The ZVS analysis is verified at various grid angles with the proposed analysis ensuring a complete ZVS operation of the ac-dc system throughout the grid cycle.

INDEX TERMS Electric vehicle (EV) charging, C_{oss} energy estimation, multi-level converter, nonlinear capacitance, resonant converter, T-type converter, unfolding-based, Unfolder, zero-voltage switching (ZVS).

I. INTRODUCTION

The surging global adoption of electric vehicles (EVs) underscores the critical demand for efficient battery chargers and accessible public charging infrastructure. Standard two-stage ac-dc converter topologies face challenges such as hard-switching of the power factor correction stage and reduced power density due to the use of large filter components [1], [2]. To overcome these limitations, recent years have witnessed the emergence of single-stage converter topologies [3]–[9], [11], [13]–[15], aiming to enhance the efficiency and power density of the converter.

One increasingly adopted single-stage topology for high-power converters is the unfolding-based ac-dc converter [6]–[15]. The 3-ϕ Unfolder circuit comprises a conventional 3-ϕ diode bridge rectifier along with a third harmonic injection network (Q_z, z $\in$ {a,b,c}), as shown in Fig. 1. Another variant of 3-ϕ Unfolder is a neutral point clamped unfolding-based rectification system as employed in [6]. The 3-ϕ

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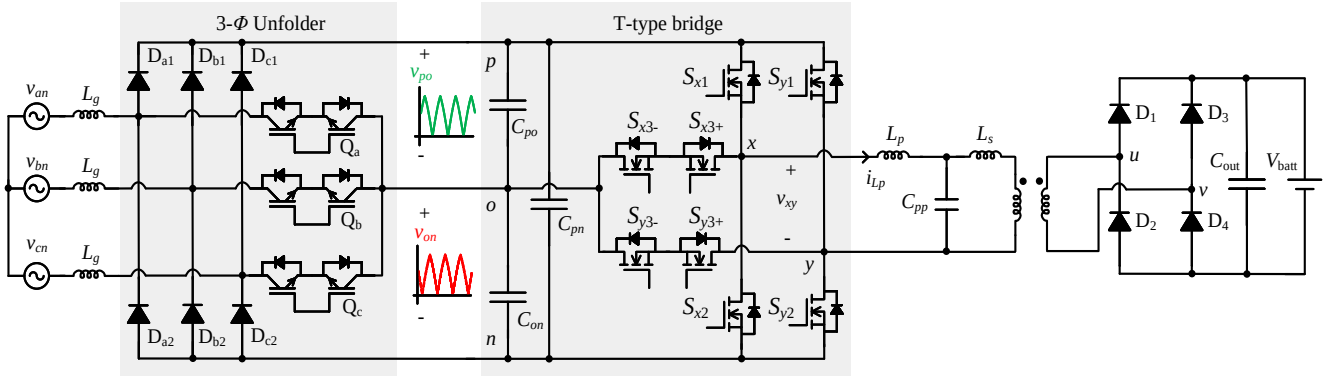

FIGURE 1. Circuit schematic of a single-stage 3-ϕ unfolding-based ac-dc conversion system comprising a 3-ϕ Unfolder-based rectifier and a T-type primary bridge-based LCL-resonant converter with passive rectification on the secondary side of the transformer.

Unfolder rectifies 3-ϕ ac voltages into two time-varying dc-link voltages, with minimal switching losses due to switching instances occurring at most twice the grid frequency. The time-varying dc-link voltages of the Unfolder can be converted into a suitable constant dc voltage by various high-frequency dc-dc converter topologies. In [6], two separate dc-dc converters are employed at the output of Unfolder, while in [7], two H-bridges feed a common secondary diode rectifier. However, each of these two dc-dc converters must be rated for peak power equal to the rated power of the 3-ϕ Unfolder. Additionally, each of these dc-dc converters has its own separate tank circuit, which results in reduced power density. Alternatively, utilizing a three-port converter like a T-type bridge requires only one high-frequency isolation transformer [9], [11]. With a well-designed soft-switched isolated dc-dc stage, the entire ac-dc conversion system can be designed to achieve high power density, high efficiency, and reduced electromagnetic interferences.

The recognized advantages of unfolding-based topologies based on T-type resonant converters have fueled their increasing adoption in EV charging applications. Despite their prevalence, conducting a thorough analysis of the soft-switching behavior in the dc-dc converter for unfolding-based applications proves challenging. This complexity is attributed to the time-varying nature of the Unfolder output voltages, compounded by the nonlinear and voltage-dependent characteristics of the output capacitance (C_{oss}) of the MOSFETs. While unfolding-based converter topologies proposed in the literature claim either complete [9], [24] or partial soft-switching [11], the specific conditions for achieving soft-switching remain unspecified. The nonlinearity associated with C_{oss} has been addressed in numerous scholarly works to estimate minimal zero-voltage switching (ZVS) energy requirements in an H-bridge [16] or half-bridge circuit [17]. However, to the best of the authors' knowledge, a comprehensive analysis of soft-switching in a T-type bridge-based resonant converter for unfolding-based applications, while incorporating the nonlinear C_{oss} effect, remains unexplored in the current literature.

ZVS is a widely adopted technique for achieving soft-switching in MOSFETs. The state-plane method has been used in the past to analyze ZVS conditions in dual active bridge converters [18]. In the context of a T-type structure, the state-plane method employed to estimate the ZVS requirements is conducted for constant dc-input voltages to the T-type bridge, fixed values of C_{oss}, and with an assumption of tank current as a constant current source [19], [20]. These factors introduce inaccuracies in the results when applied to unfolding-based ac-dc converters. In [21], zero current ZVS boundary is determined for a T-type bridge with four-level output voltage. However, the determination of accurate ZVS current when dealing with a five-level output voltage for a full-bridge T-type bridge, as utilized in this work, makes the state-plane method application notably intricate.

Another approach for ZVS analysis is the energy-based method, as adopted for a half-bridge circuit in [17]. However, a similar approach has not been employed for the ZVS analysis of a T-type bridge in the literature so far. The T-type bridge-based resonant converters in [22], [23] do not consider the energies delivered by the voltage sources while estimating ZVS energy requirements. Consequently, the minimum ZVS current derived in these works relies solely on capacitive (C_{oss}) energies. A similar assumption is noted in [24], which utilizes a T-type bridge for unfolding-based applications, and in [25] for an NPC-type three-level resonant converter. In [25], a lower ZVS range than predicted is reportedly observed during experiments. This paper demonstrates that the energy contributions from the voltage sources are not negligible. Ignoring these contributions and considering only capacitive energies leads to an underestimation of the minimum ZVS current requirement, with errors reaching up to 50%.

This work proposes an energy-based methodology to estimate the ZVS requirements of a T-type bridge for unfolding-based applications, taking into account the nonlinearity of C_{oss}. A generalized solution is offered for the minimum ZVS current and ZVS time for a T-type bridge, applicable to any resonant tank circuit. The solution is also valid for differ-

ent kinds of modulation schemes adopted in the literature including center-aligned modulation [11] and leading-edge aligned modulation [9]. Furthermore, in T-type bridge-based resonant converters, certain switching transitions may exhibit hard-switching behavior, as seen in the case of center-aligned modulation. In such cases, the C_{oss} losses are shown to be a dominant part of hard-switching losses for high-frequency wide-bandgap devices [26]. This emphasizes the necessity of analyzing the C_{oss} losses occurring in a T-type bridge during each transition separately while including the effect of nonlinear C_{oss}. This work analyses the C_{oss} energy loss in a T-type bridge during each switching transition. Furthermore, a simplified solution is presented for estimating total C_{oss} losses, proving valuable in comparing conduction losses with switching losses during the tank circuit design process.

To summarize, the major contributions of this work are listed below:

1) The minimum ZVS current and ZVS time for a T-type bridge with time-varying dc-link voltages in unfolding-based applications are determined using an energy-based method, which also considers the impact of the nonlinear, voltage-dependent C_{oss}.
2) A comprehensive analysis of the C_{oss} losses in a T-type bridge for each switching transition is conducted, and a simplified solution for calculating total C_{oss} losses is also provided.
3) The ZVS requirements have been verified on a 20-kW high-power unfolding-based hardware with a T-type bridge-based dc-dc converter. It is found that the ZVS analysis using the proposed method results in less than 1% error for ZVS current calculation and less than 5% error for ZVS time calculation.

The subsequent sections of this paper are structured as follows: Section II provides an overview of unfolding-based ac-dc converter topologies. Section III details the method for addressing the nonlinearity associated with C_{oss}. Section IV outlines the T-type bridge switching pattern and commutation process. The ZVS conditions for different switching transitions in a T-type bridge are derived in Section V. This section includes the calculation of the minimum ZVS current and ZVS time, along with C_{oss} energy loss, at each switching transition of the T-type bridge. The analysis is verified through simulation using PLECS in Section VI. Experimental results are presented in Section VII, followed by the conclusion in Section VIII.

II. Topology Description of Unfolding-Based AC-DC Converters

Fig. 1 depicts the unfolding-based ac-dc conversion system employed in this work. The 3-ϕ Unfolder circuit comprises a conventional 3-ϕ diode bridge rectifier along with a third harmonic injection network (Q_z, z $\in$ {a,b,c}). The Unfolder connects the input ac phases to the positive (p), negative (n), or midpoint node (o) of the dc-link based on the specific

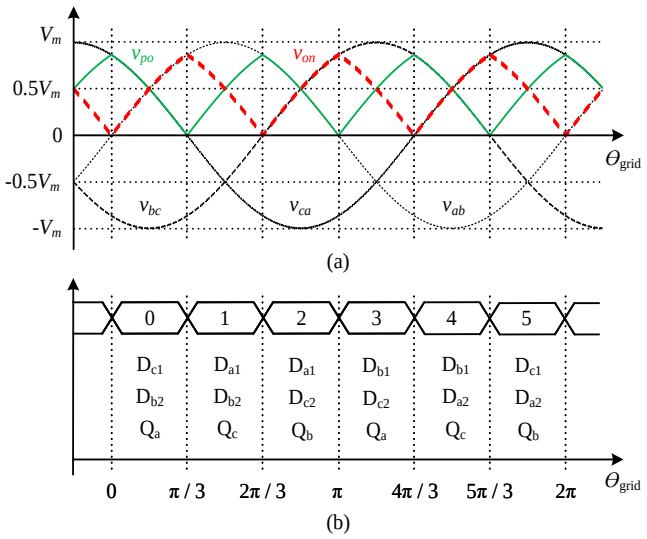

FIGURE 2. (a) 3-ϕ grid voltages and time-varying dc-link voltages, v_{po} and v_{on}, at two input ports of T-type bridge; and (b) switching sequence of the Unfolder devices as per grid voltage sectors.

switching sequence outlined in Fig. 2(b). The input phases with the maximum and minimum instantaneous voltages are linked to the p node and n node of the dc-link, respectively, while the remaining phase is linked to the o node. As a result, the injection network's switches Q_a, Q_b, and Q_c operate at twice the grid frequency, while the 3-ϕ rectifier switches D_{a1}, D_{a2}, D_{b1}, D_{b2}, D_{c1}, and D_{c2} operate at the grid frequency, resulting in negligible switching losses in the Unfolder circuit. The switching scheme of the Unfolder results in two time-varying dc-link voltages at its output, as illustrated in Fig. 2(a). The time-varying dc-link voltage across the nodes p and o is termed as v_{po}, and across the nodes o and n is termed as v_{on}. These time-varying voltages can be expressed as

$$v_{po}(\theta_{\text{grid}}) = \begin{cases} V_m \sin\left(\theta_{\text{grid}} + \frac{2(k+1)\pi}{3}\right) & \text{for even } k; \\ V_m \sin\left(\theta_{\text{grid}} + \frac{(2k+3)\pi}{3}\right) & \text{for odd } k; \end{cases} \quad (1)$$

and

$$v_{on}(\theta_{\text{grid}}) = \begin{cases} V_m \sin\left(\theta_{\text{grid}} + \frac{2k\pi}{3}\right) & \text{for even } k; \\ V_m \sin\left(\theta_{\text{grid}} + \frac{(2k-1)\pi}{3}\right) & \text{for odd } k; \end{cases} \quad (2)$$

Here, the grid angle, θ_{grid}, for the k^{th} Unfolder sector varies within the range $\frac{k\pi}{3} \leq \theta_{\text{grid}} \leq \frac{(k+1)\pi}{3}$, and V_m represents the peak of 3-ϕ line-to-line input voltages. The voltages v_{po} and v_{on} vary from 0 to $\frac{\sqrt{3}V_m}{2}$. To process the power from the two output ports of the Unfolder, either two dc-dc converters or a single three-port dc-dc converter capable of handling two input voltages is essential. This work adopts a three-port T-type bridge-based dc-dc converter, chosen for its noted advantages in terms of power density and efficiency.

This work focuses on Unfolder sector '0', where θ_{grid} varies from 0 to $\frac{\pi}{3}$, for conducting ZVS analysis of the T-type bridge. However, it is important to note that the

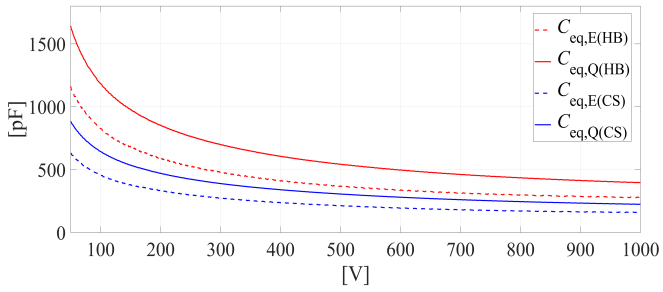

FIGURE 3. Charge and energy-equivalent capacitance values for drain-to-source voltage variation from 0 V to 1000 V for two of the Omsemi SiC MOSFETs employed in this work, represented by solid and dotted lines, respectively.

presented analytical approach can be applied to other sectors. The time-varying output voltages of the Unfolder are two input voltages for the T-type bridge. The time-varying nature of these voltages introduces complexities in analyzing ZVS conditions due to the nonlinear and voltage-dependent nature of the MOSFETs C_{oss}. Therefore, the subsequent section is dedicated to first addressing the nonlinearity of C_{oss}.

III. Nonlinear C_{oss} Equivalents

Semiconductor devices exhibit capacitance between their various terminals due to the depletion region formed at their junctions. For MOSFETs, C_{oss} is a nonlinear function of the drain-to-source voltage (v_{ds}). This voltage dependence varies among different semiconductor technologies and manufacturers' device implementation techniques. Although there are several SPICE model-based approaches documented in the literature [27], [28], it is often challenging to fit all these curves with a general empirical curve-fit formula, especially for modern devices with complex structures such as wide-band-gap or super junction devices. Therefore, defining an equivalent capacitance value that stores the same amount of charge or energy for a given voltage change proves to be valuable. If $C_{\text{oss}}|_v$ represents the C_{oss} value evaluated at a voltage v, the charge stored in C_{oss} can be described by

$$\mathrm{d}q_C = C_{\text{oss}}|_v \, \mathrm{d}v \tag{3}$$

in the small signal domain, where $\mathrm{d}q_C$ is a small signal change in the charge for a voltage change of $\mathrm{d}v$. As C_{oss} is a function of voltage v, integration must be performed to calculate the total charge accumulated. The total charge Q_c accumulated while charging C_{oss} from 0 to v_c is

$$Q_c\Big|_0^{v_c} = \int_0^{v_c} C_{\text{oss}}|_v \, \mathrm{d}v. \tag{4}$$

Similarly, the energy stored when charging C_{oss} from 0 to v_c, denoted as E_c, is

$$E_c\Big|_0^{v_c} = \int_0^{v_c} v \, C_{\text{oss}}|_v \, \mathrm{d}v. \tag{5}$$

Due to the nonlinearity involved, numerical integration must be performed. As the nonlinearity cannot be correctly modeled in terms of time, energy, and charge simultaneously using a single capacitance value, the energy-equivalent capacitance denoted by $C_{\text{eq,E}}$, and charge-equivalent capacitance denoted by $C_{\text{eq,Q}}$ are introduced [16]. These charge and energy-equivalent capacitance values are

$$C_{\text{eq,Q}}\Big|_0^{v_c} = \frac{1}{v_c}\int_0^{v_c} C_{\text{oss}}|_v \, \mathrm{d}v, \tag{6}$$

$$C_{\text{eq,E}}\Big|_0^{v_c} = \frac{2}{{v_c}^2}\int_0^{v_c} v \, C_{\text{oss}}|_v \, \mathrm{d}v. \tag{7}$$

Here, the energy stored in $C_{\text{eq,E}}$ at voltage v_c is the same as energy stored when the voltage across C_{oss} changes from 0 to v_c. Similarly, the charge stored in $C_{\text{eq,Q}}$ at voltage v_c is the same as the charge stored when charging C_{oss} from 0 to v_c, where v_c can be any value from 0 to rated operating voltage of the MOSFET.

To compute the charge-equivalent capacitance in the scenario where C_{oss} charges from v_1 to v_2, the initial step involves calculating the total charge, given as

$$\begin{aligned} Q_c\Big|_{v_1}^{v_2} &= \int_0^{v_2} C_{\text{oss}}|_v \, \mathrm{d}v - \int_0^{v_1} C_{\text{oss}}|_v \, \mathrm{d}v, \\ Q_c\Big|_{v_1}^{v_2} &= C_{\text{eq,Q}}\Big|_0^{v_2} v_2 - C_{\text{eq,Q}}\Big|_0^{v_1} v_1. \end{aligned} \tag{8}$$

This provides the charge-equivalent capacitance value when C_{oss} charges from v_1 to v_2 as

$$C_{\text{eq,Q}}\Big|_{v_1}^{v_2} = \frac{C_{\text{eq,Q}}\Big|_0^{v_2} v_2 - C_{\text{eq,Q}}\Big|_0^{v_1} v_1}{v_2 - v_1}, \tag{9}$$

where v_1 and v_2 can be any values from 0 to the rated operating voltage of the MOSFET. Fig. 3 shows the charge and energy-equivalent capacitances calculated for two of the 1200 V Omsemi Silicon Carbide (SiC) MOSFETs employed in this work, details of which are provided in the experimental section. These values are calculated at various drain-to-source voltages ranging from 0 V to 1000 V. To create these curves, data points are extracted from the C_{oss} - v_{ds} curves provided in the datasheets [29], [30], and numerical integration is performed in MATLAB as provided in Appendix A. In Fig. 3, the term $C_{\text{eq,Q(HB)}}$ represents the charge-equivalent capacitance for half-bridge switches (S_{x1}, S_{x2}, S_{y1}, and S_{y2}) and $C_{\text{eq,Q(CS)}}$ represents the charge-equivalent capacitance for common-source switches (S_{x3+}, S_{x3-}, S_{y3+}, and S_{y3-}).

Furthermore, the C_{oss} variation with external factors such as temperature, gate-to-source voltage, and any tolerance (if known) for the specific device technologies should be considered when calculating equivalent capacitance values [31]–[33]. Finally, using these equivalent capacitances, the time-varying nature of dc-link voltages can be handled during ZVS analysis. Before delving into the ZVS analysis, Section IV first provides a thorough exploration of the T-type bridge switching pattern and the charging-discharging process of the C_{oss} within a switching cycle.

IV. T-type Bridge Switching and Commutation Pattern

In comparison to a two-level half-bridge structure, a T-type bridge leg incorporates two additional series-connected

TABLE 1. Possible switch states and corresponding voltage v_{xy}.

S_{x1} ($\overline{S_{x3+}}$)	S_{x2} ($\overline{S_{x3-}}$)	S_{y1} ($\overline{S_{y3+}}$)	S_{y2} ($\overline{S_{y3-}}$)	v_{xy}
0	0	0	0	0
0	0	0	1	v_{on}
0	0	1	0	$-v_{po}$
0	1	0	0	$-v_{on}$
0	1	0	1	0
0	1	1	0	$-v_{pn}$
1	0	0	0	v_{po}
1	0	0	1	v_{pn}
1	0	1	0	0

common-source switches between the switch nodes (x node or y node) and the midpoint (o node) of the input dc-link. For the x leg, the switches S_{x1} and S_{x2} need to block total dc-link voltage across the p node to n node, whereas common-source switches, S_{x3+} and S_{x3-} combined only need to block the voltage across one of the input ports (either v_{po} or v_{on}) at a given instant. A similar statement can be made for the y leg. The switches S_{x1}, S_{x3+}, S_{y1}, and S_{y3+} are collectively responsible for applying $\pm v_{po}$ voltages across switch nodes x and y. Additionally, the remaining four switches apply $\pm v_{on}$ voltages across the switch nodes x and y.

There are several ways to generate a switching pattern for a T-type bridge. However, to prevent a short circuit condition in the dc-link, it is imperative to ensure that the switches S_{z1} and S_{z2}, $z \in \{x, y\}$, are never simultaneously turned on within one leg. With this constraint, the possible states of the switch node voltage v_{xy} are listed in TABLE 1, where the switch state '0' represents 'off', and '1' represents 'on'. As observed from TABLE 1, there are a total of six possible active states and three possible zero-states.

Out of the various switching patterns that can be derived from TABLE 1, one possible switching pattern is shown in Fig. 4, along with the T-type bridge switch node voltage v_{xy}. In Fig. 4, T_s denotes one complete switching period of the converter.

The duty ratios, d_p and d_n, correspond to the durations for which v_{po} and v_{on}, respectively, are applied at the T-type bridge output. Both d_p and d_n can vary from 0 to 1. The analysis in this section considers commutation sequence specific to the case when $v_{on} \geq v_{po}$ which is the case for grid angle $\frac{\pi}{6} \leq \theta_{\text{grid}} \leq \frac{\pi}{3}$ for Unfolder sector '0', as can be seen from Fig. 2. The analysis is similar for the other case with $v_{po} \geq v_{on}$, and it is omitted for brevity. The switching patterns depicted in Fig. 4 reveal that each T-type bridge leg undergoes four switching transitions (I, II, III, and IV). Transition I is defined as the transition during which the switch node of leg x transitions from the n node to the o node. Other transitions are defined similarly and shown in Fig. 4.

The previous literature outlines modulation strategies for T-type bridges based on various switching patterns. These strategies include leading-edge aligned modulation [9],

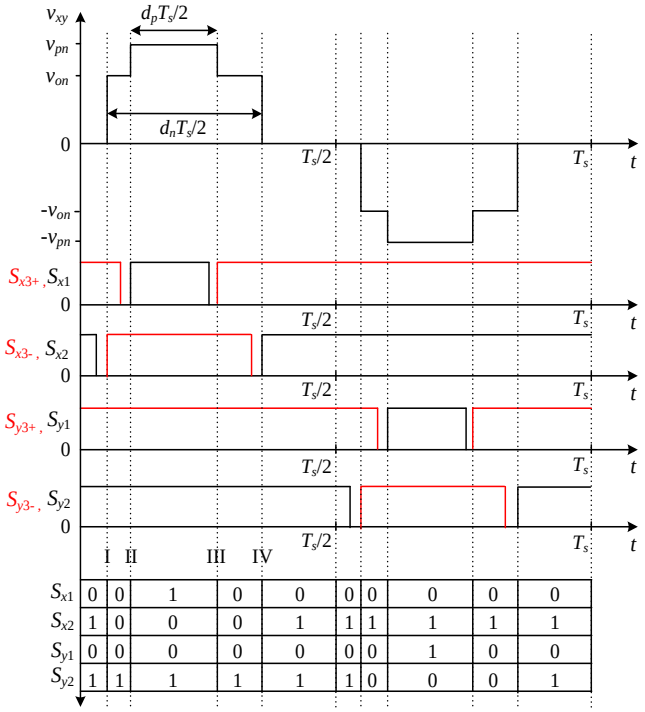

FIGURE 4. The switching pattern for the T-type bridge with a five-level output voltage, v_{xy}.

where the leading edges of the quasi-square voltage waveforms generated corresponding to voltages v_{po} and v_{on} are aligned, and center-aligned modulation [11], where the two waveforms are center-aligned. To minimize the inductive loading of the tank circuit while ensuring ZVS for all switching transitions, aligning transition I and transition II is beneficial, resulting in leading-edge aligned modulation. However, this alignment causes a direct transition of the switch node of leg x from the n node to the p node, resulting in incomplete soft-switching of common-source switches, as elaborated in [9]. Therefore, this work adopts leading-edge aligned modulation with a delay time termed as the staggering time (approximately equal to the dead time) provided between transition I and transition II. It is worth noting that the need for such staggering time arises from the unequal input voltages in the case of unfolding-based converters.

To understand the T-type switching transitions, each switching transition for leg x is analyzed separately. The switching transitions of leg y are also similar and they are skipped for brevity. In Fig. 5 and Fig. 6, the switches that are turned on are shown in black, and the switches that are turned off are shown in gray. The active section of the circuit, where the current is flowing, is highlighted in red.

A. Transition I (n to o node)

During transition I, as shown in Fig. 5(a), the switch S_{x2} initially turns off. Since there is no path for the C_{oss} of S_{x2} to charge with an open-circuited tank, the circuit remains

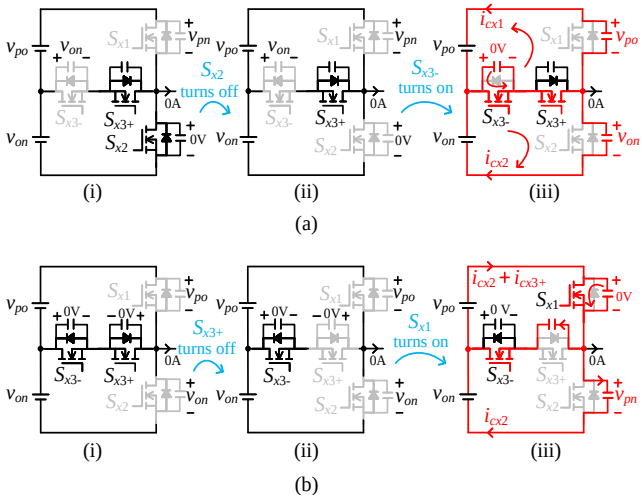

FIGURE 5. **Commutation process involving charging and discharging of C_{oss} of MOSFETs during (a) transition I, (b) transition II with zero tank current. The circuits in (a) and (b) represent the time (i) before the device turns off, (ii) during the dead time, and (iii) after the complementary device turns on.**

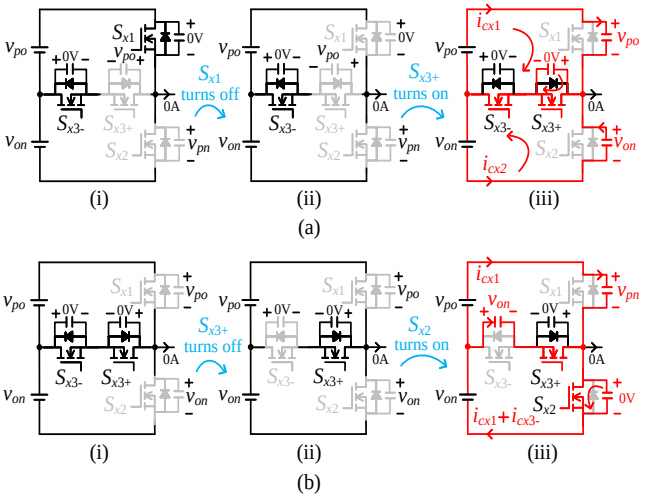

FIGURE 6. **Commutation process involving charging and discharging of C_{oss} of MOSFETs during (a) transition III, (b) transition IV with zero tank current. The circuits in (a) and (b) represent the time (i) before the device turns off, (ii) during the dead time, and (iii) after the complementary device turns on.**

unchanged in Fig. 5(a)(i) and (ii). After the dead time, $S_{x3\text{-}}$ turns on, and its C_{oss} discharges through its own channel. This also allows the C_{oss} of S_{x2} to charge from 0 to v_{on}. Simultaneously, switch S_{x1}, which is already off, discharges from v_{pn} to v_{po}.

B. Transition II (o to p node)

During transition II, as shown in Fig. 5(b), switch S_{x1} discharges completely from v_{po} to 0, connecting the switch node x to p node. Switch S_{x3+} charges from 0 to v_{po}, and switch S_{x2} charges from v_{on} to v_{pn}. It is crucial to note that despite the switch S_{x2} remaining off during transition II, it continues to charge. Therefore, an additional commutation loop is present during each switching transition in the case of a T-type bridge. This observation holds true for all other transitions as well.

TABLE 2. **C_{oss} charging and discharging during different transitions.**

Transition	S_{x1}	S_{x2}	S_{x3+}	S_{x3-}
I (n to o node)	v_{pn} to v_{po}	0 to v_{on}	-	v_{on} to 0
II (o to p node)	v_{po} to 0	v_{on} to v_{pn}	0 to v_{po}	-
III (p to o node)	0 to v_{po}	v_{pn} to v_{on}	v_{po} to 0	-
IV (o to n node)	v_{po} to v_{pn}	v_{on} to 0	-	0 to v_{on}

C. Transition III (p to o node)

In Fig. 6(a), switching transition III is shown, where the transition from the p node to the o node takes place with S_{x1} charging and S_{x3+} discharging from v_{po} to 0. As previously mentioned, an additional commutation loop due to the discharging of non-active device S_{x2} can be observed.

D. Transition IV (o to n node)

In Fig. 6(b) switching transition IV is depicted, during which switch S_{x2} discharges completely from v_{on} to 0, connecting switch node x to the n node.

TABLE 2 summarizes the changes in voltages of the MOSFET capacitances for these four transitions. With an established understanding of the charging and discharging process of MOSFETs involving nonlinear C_{oss} and the commutation sequence of the T-type bridge, energy-based ZVS analysis can be introduced in the next section.

V. ZVS Requirements For the T-type Bridge

A. Minimum ZVS current requirement

The equivalent circuits during dead times for all four transitions are shown in Fig. 7. Here, the LCL tank circuit depicted in Fig. 1 is replaced by an equivalent circuit consisting of inductor L_p and a voltage source v_{Cpp}. The voltage source v_{Cpp} represents the instantaneous capacitor voltage of C_{pp} during the switching transition under study. The voltage across the capacitor remains relatively constant during the dead time and is treated as a constant voltage source for ZVS analysis. However, different values of v_{Cpp} for different switching transitions as well as the variation of v_{Cpp} over the grid cycle are considered. It is important to note that a similar equivalent circuit can be obtained for any other type of resonant tank circuit; hence, the ZVS analysis remains applicable for all types of resonant tank circuits. The transition I and transition II are investigated thoroughly to establish the ZVS requirements. For achieving ZVS for the x leg, current going into the switch node x is required for transition I and II, whereas current going out of the switch node x is required for transition III and IV. To calculate the energy required from tank inductance L_p, the energies of each component in the circuit are calculated, and the energy

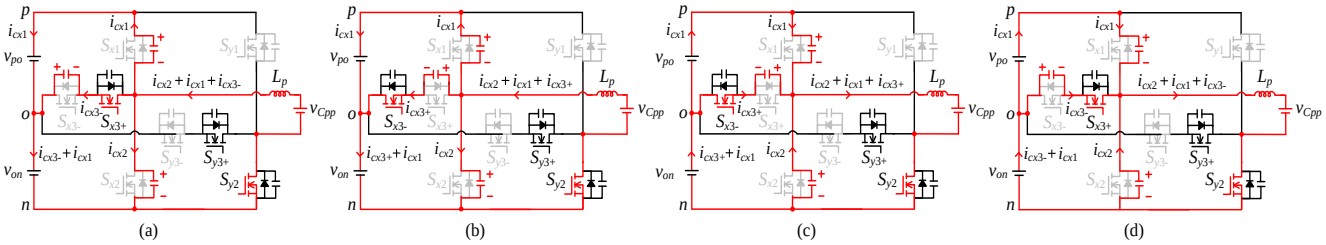

FIGURE 7. Commutation with ZVS during the dead time at (a) transition I (*n* node to *o* node), (b) transition II (*o* node to *p* node), (c) transition III (*p* node to *o* node), and (d) transition IV (*o* node to *n* node).

conservation equation [17], given by

$$E_{c,\text{initial}} + E_{\text{delivered}} = E_{c,\text{final}} + E_{\text{dissipated}}, \tag{10}$$

is employed. Here, $E_{c,\text{initial}}$ is the total initial capacitive (C_{oss}) energy in the circuit before the particular switching transition and $E_{c,\text{final}}$ is the total final capacitive energy in the circuit after the switching transition. The terms $E_{\text{delivered}}$ and $E_{\text{dissipated}}$ denote the total energy delivered and the total energy dissipated in the circuit during the switching transition, respectively. This section will demonstrate that the energies associated with the two input sources, v_{po} and v_{on}, and the reflected tank voltage, v_{Cpp}, are significant and cannot be ignored.

1) Transition I (*n* node to *o* node)

During transition I, switches S_{x1}, S_{x2}, and $S_{x3\text{-}}$ of x leg remain in active commutation loops. Meanwhile, with the switch S_{y2} turned on, the switch node y is tied to the n node of the dc-link. To achieve ZVS during transition I, the current going into the leg x is necessary. From Fig. 7(a), it is evident that the current i_{cx1} flowing through the source v_{po} is the same as the discharging current of switch S_{x1}. Consequently, the energy delivered by the source v_{po} denoted as $E_{v_{po}}$, can be calculated as

$$E_{v_{po}} = -\int i_{cx1} v_{po} dt = -C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} v_{po} v_{on}, \tag{11}$$

The negative sign for $E_{v_{po}}$ indicates that the source absorbs energy during the transition. The energies delivered by the other two sources can also be calculated in a similar manner. The energies delivered by the input voltage source v_{on} and reflected tank voltage source v_{Cpp} are

$$E_{v_{on}} = -v_{on}^2 \left(C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{on}} \right), \tag{12}$$

$$E_{v_{Cpp}} = v_{Cpp} v_{on} \left(C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{on}} + C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{on}} \right). \tag{13}$$

The total energy delivered by the three sources and the inductor during the switching process can be written as

$$E_{(\text{delivered})} = E_{L_p} + E_{v_{Cpp}} + E_{v_{po}} + E_{v_{on}}. \tag{14}$$

For complete ZVS, the energy dissipated in the circuit is zero ($E_{\text{dissipated}} = 0$), and using (10), the energy that needs

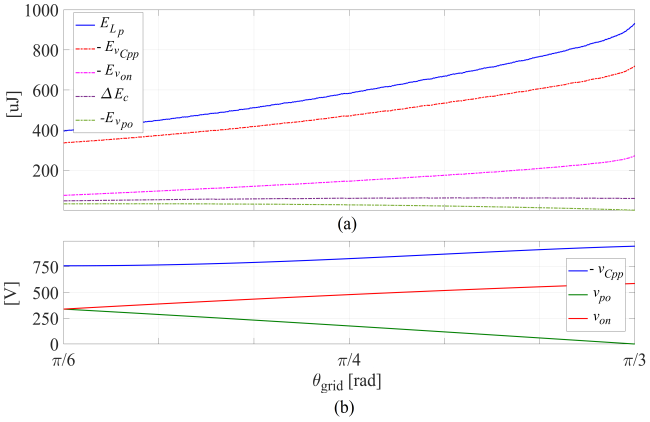

FIGURE 8. (a) Energies delivered by v_{po}, v_{on}, and v_{Cpp} (with negative signs denoting energy absorption), the contribution of change in capacitive (C_{oss}) energy ΔE_c, and total energy required from the inductor L_p during switching transition I as a function of θ_{grid}, (b) time-varying input voltages v_{po}, v_{on}, and reflected tank voltage v_{Cpp}.

to be processed by the inductance L_p is

$$E_{L_p(\text{trI})} = -E_{v_{Cpp}} - E_{v_{po}} - E_{v_{on}} - \Delta E_c, \tag{15}$$

where ΔE_c is the total change in capacitive energy during the switching transition. From TABLE 2, the total change in the capacitive energy during transition I is

$$\begin{aligned} \Delta E_c &= E_{c,\text{initial}} - E_{c,\text{final}} \\ &= \frac{1}{2} C_{\text{eq,E(HB)}}\Big|_{0}^{v_{pn}} v_{pn}^2 - \frac{1}{2} C_{\text{eq,E(HB)}}\Big|_{0}^{v_{po}} v_{po}^2 \\ &\quad + \frac{1}{2}\left(C_{\text{eq,E(CS)}}\Big|_{0}^{v_{on}} - C_{\text{eq,E(HB)}}\Big|_{0}^{v_{on}} \right) v_{on}^2. \end{aligned} \tag{16}$$

If v_{Cpp} is negative during transition I, as is typically the case for forward power flow direction, the term $E_{v_{Cpp}}$ in (13) is negative. Consequently, all the terms $E_{v_{po}}$, $E_{v_{on}}$ and $E_{v_{Cpp}}$ are negative in (11)-(13), as all sources are absorbing energy during transition I. These energies must be provided by L_p in addition to the change in capacitive energy required.

Fig. 8 illustrates the energies absorbed by v_{po}, v_{on}, and v_{Cpp} as a function of θ_{grid} within a specific Unfolder sector (sector '0': $0 < \theta_{\text{grid}} < \pi/3$). It is important to note that the contributions of the voltage sources play a pivotal role in determining the minimum energy demand from inductor L_p. The overall change in capacitive energy during the transition, denoted as ΔE_c, remains notably minimal and, in fact, reduces the energy requirement for ZVS from the

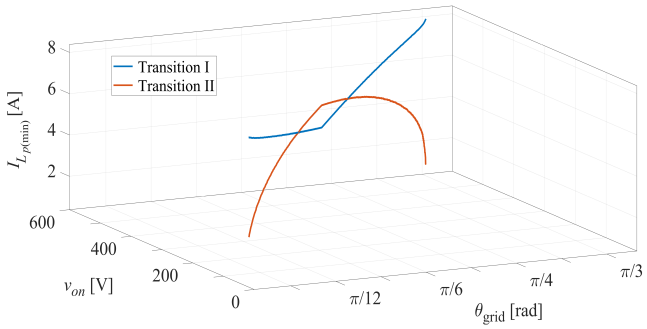

FIGURE 9. **Variation of minimum ZVS current required as a function of θ_{grid} and input voltage v_{on} during transition I and transition II.**

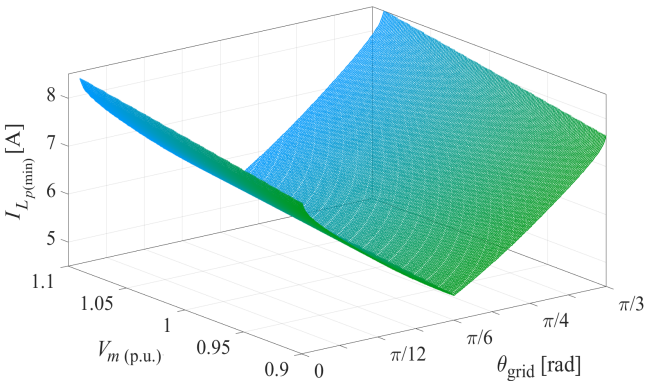

FIGURE 10. **Minimum ZVS current variation for transition I as a function of θ_{grid}, with $\pm 10\%$ variation in the grid voltage.**

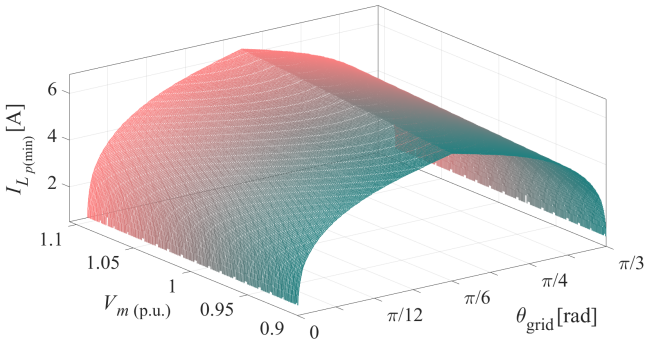

FIGURE 11. **Minimum ZVS current variation for transition II as a function of θ_{grid}, with $\pm 10\%$ variation in the grid voltage.**

inductor L_p. This observation is not limited to unfolding-based topologies; it holds true even when constant input voltages are applied to the T-type bridge.

It can further be seen from Fig. 7(a) and Fig. 7(d) that transitions I and IV are identical except for the direction of currents. Hence the minimum ZVS current condition is the same for the transition from *n* node to *o* and vice-versa.

2) Transition II (*o* node to *p* node)

A similar process can be adopted for the transition II. The energies delivered by the three sources during transition II can be calculated as

$$E_{v_{po}} = -v_{po}^2 C_{\text{eq,Q(HB)}}\Big|_0^{v_{po}}, \tag{17}$$

$$E_{v_{on}} = -v_{on} v_{po}\Big(C_{\text{eq,Q(HB)}}\Big|_0^{v_{po}} + C_{\text{eq,Q(CS)}}\Big|_0^{v_{po}}\Big). \tag{18}$$

$$E_{v_{Cpp}} = v_{Cpp} v_{po}\Big(C_{\text{eq,Q(HB)}}\Big|_{v_{on}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_0^{v_{po}} + C_{\text{eq,Q(HB)}}\Big|_0^{v_{po}}\Big), \tag{19}$$

Equation (15) can be used again to find $E_{L_p(\text{trII})}$, where ΔE_c for transition II can be calculated using TABLE 2. Finally, the minimum current for ZVS during a particular switching transition in a T-type bridge can be calculated as

$$I_{L_p(\min)} = \left| \sqrt{\frac{2E_{L_p}}{L_p}} \right|, \tag{20}$$

where E_{L_p} for transition I (or IV) is $E_{L_p(\text{trI})}$ given by (15), and for transition II (or III) can be calculated using (15) and (17)-(19). In cases where E_{L_p} is negative or zero, no minimum energy requirement exists and ZVS is achieved if adequate dead time is provided.

The variation in the minimum ZVS current during transition I and transition II can be observed, along with the time-varying input voltage v_{on}, in Fig. 9 for the Unfolder sector '0' with L_p = 29.3 μH. Moreover, in unfolding-based ac-dc converter topologies, any fluctuations in the 3-ϕ grid input are directly seen at the input of the T-type bridge, consequently influencing the minimum ZVS current requirement. For the development of a well-designed converter, due consideration must be given to this aspect. This variation is illustrated in Fig. 10 and Fig. 11 for transition I and transition II, respectively, where the minimum ZVS current variations are presented under $\pm 10\%$ fluctuation in the 3-ϕ grid voltage. Such challenges are not present in a typical T-type bridge with constant input dc voltages.

B. ZVS time requirement

In addition to the minimum ZVS current requirement, determining the time necessary for achieving ZVS of the MOSFETs during the switching transitions is also a crucial parameter for resonant converters. This calculation plays a key role in establishing the appropriate dead time to ensure that MOSFETs do not turn on prematurely before the complete discharge of their C_{oss}. As discussed earlier, in the context of the T-type bridge-based resonant converter in unfolding-based topologies, the minimum ZVS currents required vary based on T-type input voltages, v_{po} and v_{on}, which are functions of θ_{grid}. Consequently, the ZVS time also exhibits variations throughout the grid cycle, unlike typical resonant converters operating with fixed input dc voltages. The analysis here considers that the tank current during the transitions is maintained at the minimum ZVS current level, as given by (20). Nonetheless, this analysis is also expanded to accommodate scenarios where the tank current during the transitions exceeds the minimum requirement.

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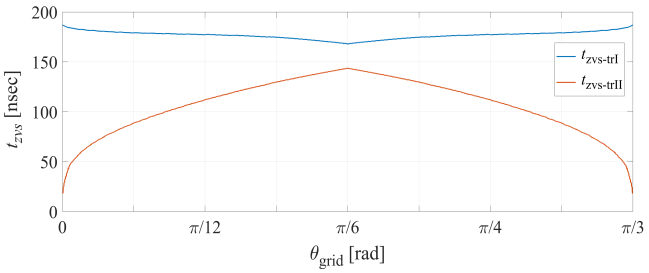

FIGURE 12. Variation in ZVS times over the grid cycle as a function of θ_{grid} for transition I and transition II.

The determination of the ZVS time for the transition I involves the application of Kirchhoff's Current Law (KCL) at the node x in Fig. 7(a), expressed as

$$\begin{aligned} i_{L_p} &= -i_{cx1} - i_{cx2} - i_{cx3-}\,, \\ &= C_{\text{oss-}x1}\frac{\mathrm{d}v_{ds\text{-}x1}}{\mathrm{d}t} - C_{\text{oss-}x2}\frac{\mathrm{d}v_{ds\text{-}x2}}{\mathrm{d}t} + C_{\text{oss-}x3\text{-}}\frac{\mathrm{d}v_{ds\text{-}x3-}}{\mathrm{d}t}\,. \end{aligned} \tag{21}$$

From (21), the charge needed by the MOSFETs' C_{oss} can be equated to the charge supplied by the tank current, i_{L_p}, essentially representing the area under the current waveshape. The computation of the time requirement is then expressed as

$$t_{\text{zvs-trI}} = \frac{2\,v_{on}\left(C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{on}} + C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{on}}\right)}{I_{L_p(\text{min-trI})}}. \tag{22}$$

A similar analysis can be done for transition II to calculate the corresponding ZVS time as

$$t_{\text{zvs-trII}} = \frac{2\,v_{po}\left(C_{\text{eq,Q(HB)}}\Big|_{v_{on}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{po}} + C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{po}}\right)}{I_{L_p(\text{min-trII})}}. \tag{23}$$

The variation of the ZVS times required during the transitions I and II for $\theta_{\text{grid}} = 0$ to $\frac{\pi}{3}$ is depicted in Fig. 12. The repetitive nature of this variation pattern extends to the remaining grid angles. The figure indicates that a dynamic adjustment of dead time throughout the grid cycle is essential to mitigate the occurrence of partial ZVS. Alternatively, a more straightforward strategy involves setting the dead time to the maximum required ZVS time, at the cost of increased conduction losses through the body diodes of the MOSFETs. As mentioned earlier, if the tank current exceeds the minimum ZVS current requirements for transitions I and II as depicted in Fig. 9, (22) and (23) can be modified to the equations provided at the bottom of the page. In (28) and (29), $I_{L_p\text{-}m}$ represents the peak of the tank current, and ω_s denotes the angular switching frequency of operation.

Lastly, Fig. 13 presents a flowchart detailing the process of determining the minimum ZVS current and ZVS time in a T-type bridge as described in this paper.

C. Estimation of C_{oss} energy losses

Insufficient tank inductor energy or ZVS time to achieve ZVS in a particular switching transition leads to either partial soft-switching or complete hard-switching. To provide a complete analysis, this section outlines the energy loss due to C_{oss} for each switching transition, focusing on the scenario of hard-switching. For this, tank current i_{L_p} is assumed to be zero, as shown by Fig. 5 and Fig. 6. A thorough explanation of the energy loss calculation during switching transition I is presented, while the details for other transitions are tabulated in TABLE 3.

During switching transition I, the current flows through the channels of switches S_{x3+} and $S_{x3\text{-}}$, leading to energy losses in channels of these switches. The energy loss happening during the switching process can be calculated by using the energy conservation expression given in (10). The energies delivered by the two sources v_{po} and v_{on} can be calculated as

$$E_{v_{po}} = -\int i_{cx1}v_{po}dt = -C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} v_{po}v_{on}, \tag{24}$$

$$E_{v_{on}} = \int i_{cx2}v_{on}dt = C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{on}} v_{on}^2. \tag{25}$$

The negative sign for $E_{v_{po}}$ indicates that the source absorbs energy during the transition. The total energy delivered during transition I is then calculated as

$$E_{\text{delivered}} = E_{v_{po}} + E_{v_{on}}. \tag{26}$$

The total energy loss or energy dissipation occurring during the transition I can be determined as

$$E_{\text{dissipated(trI)}} = E_{v_{po}} + E_{v_{on}} + \Delta E_c, \tag{27}$$

where ΔE_c is given in TABLE 3, and $E_{v_{po}}$ and $E_{v_{on}}$ are given by (24) and (25), respectively. Similarly, energy losses during the remaining three transitions can be calculated using the expressions listed in TABLE 3. The total C_{oss} energy loss during one switching period, obtained by summing all

$$t_{\text{excess-zvs-trI}} = \frac{I_{L_p(\text{trI})} - \sqrt{I_{L_p(\text{trI})}^2 - 2\,\omega_s I_{L_p\text{-}m}v_{on}\left(C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{on}} + C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{on}}\right)}}{\omega_s I_{L_p\text{-}m}}, \tag{28}$$

$$t_{\text{excess-zvs-trII}} = \frac{I_{L_p(\text{trII})} - \sqrt{I_{L_p(\text{trII})}^2 - 2\,\omega_s I_{L_p\text{-}m}v_{po}\left(C_{\text{eq,Q(HB)}}\Big|_{v_{on}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{po}} + C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{po}}\right)}}{\omega_s I_{L_p\text{-}m}}. \tag{29}$$

TABLE 3. Summary of energy contributions from two sources and the change in total capacitive energy in the *x*-leg of a T-type circuit at various transitions (Tr) when estimating $C_{\rm oss}$ energy losses for a T-type bridge.

Tr	$E_{v_{po}}$	$E_{v_{on}}$	$\Delta E_c = E_{c,\text{initial}} - E_{c,\text{final}}$
I	$-C_{\text{eq,Q(HB)}}\Big\|_{v_{po}}^{v_{pn}} v_{po}v_{on}$	$C_{\text{eq,Q(HB)}}\Big\|_{0}^{v_{on}} v_{on}^2$	$\frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{pn}} v_{pn}^2 - \frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{po}} v_{po}^2 + \frac{1}{2}\left(C_{\text{eq,E(CS)}}\Big\|_{0}^{v_{on}} - C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{on}}\right)v_{on}^2$
II	$\left(C_{\text{eq,Q(HB)}}\Big\|_{v_{on}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big\|_{0}^{v_{po}}\right)v_{po}^2$	$C_{\text{eq,Q(HB)}}\Big\|_{v_{on}}^{v_{pn}} v_{on}v_{po}$	$\frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{on}} v_{on}^2 - \frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{pn}} v_{pn}^2 + \frac{1}{2}\left(C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{po}} - C_{\text{eq,E(CS)}}\Big\|_{0}^{v_{po}}\right)v_{po}^2$
III	$C_{\text{eq,Q(HB)}}\Big\|_{0}^{v_{po}} v_{po}^2$	$-C_{\text{eq,Q(HB)}}\Big\|_{v_{on}}^{v_{pn}} v_{on}v_{po}$	$\frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{pn}} v_{pn}^2 - \frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{on}} v_{on}^2 + \frac{1}{2}\left(C_{\text{eq,E(CS)}}\Big\|_{0}^{v_{po}} - C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{po}}\right)v_{po}^2$
IV	$C_{\text{eq,Q(HB)}}\Big\|_{v_{po}}^{v_{pn}} v_{po}v_{on}$	$\left(C_{\text{eq,Q(HB)}}\Big\|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q(CS)}}\Big\|_{0}^{v_{on}}\right)v_{on}^2$	$\frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{po}} v_{po}^2 - \frac{1}{2}C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{pn}} v_{pn}^2 + \frac{1}{2}\left(C_{\text{eq,E(HB)}}\Big\|_{0}^{v_{on}} - C_{\text{eq,E(CS)}}\Big\|_{0}^{v_{on}}\right)v_{on}^2$

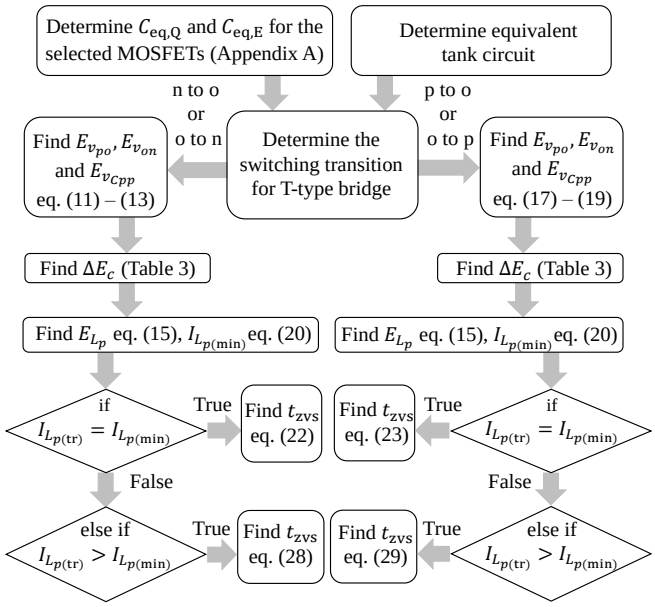

FIGURE 13. Flowchart depicting the process to determine ZVS current and ZVS time for the T-type bridge.

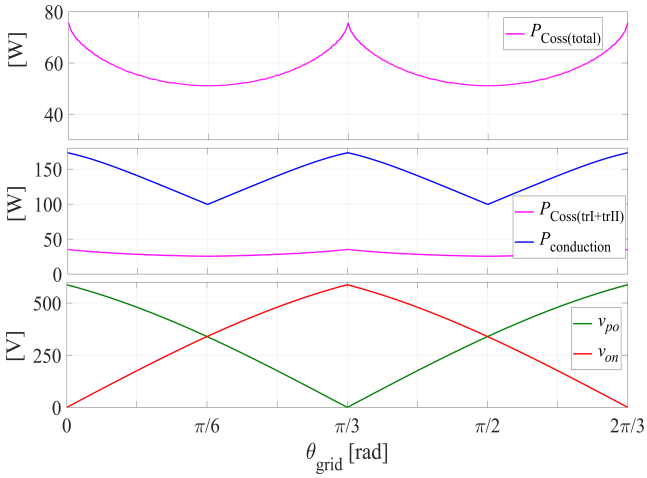

FIGURE 14. (a) Variation of total $C_{\rm oss}$-based switching loss, denoted by $P_{\text{Coss(total)}}$, as a function of θ_{grid} for 85 kHz switching frequency, (b) total conduction losses in the T-type bridge ($P_{\text{conduction}}$) and combined $C_{\rm oss}$-based switching loss for transition I and transition II ($P_{\text{Coss(trI+trII)}}$), and (c) the corresponding variations of two time-varying voltages v_{po} and v_{on} with θ_{grid}.

the losses calculated at different switching transitions and adding a factor of two for incorporating y leg energy loss, is

$$\begin{aligned} E_{\text{loss}} = {} & 2\left(C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{on}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{on}}\right)v_{on}^2 \\ & + 2\left(C_{\text{eq,Q(HB)}}\Big|_{0}^{v_{po}} + C_{\text{eq,Q(CS)}}\Big|_{0}^{v_{po}}\right)v_{po}^2 \\ & + 2\,C_{\text{eq,Q(HB)}}\Big|_{v_{po}}^{v_{pn}} v_{on}^2 + 2C_{\text{eq,Q(HB)}}\Big|_{v_{on}}^{v_{pn}} v_{po}^2. \end{aligned} \quad (30)$$

Equation (30) reveals that the total $C_{\rm oss}$ energy loss is solely dependent on the charge-equivalent capacitance and is independent of the energy-equivalent capacitance. Thus, using (30) alone is adequate for calculating total $C_{\rm oss}$ energy loss. Alternatively, (30) can be directly derived from TABLE 2 by identifying the switches involved in charging.

Fig. 14(a) shows the variation of total $C_{\rm oss}$-based switching loss, denoted by $P_{\text{Coss(total)}}$, as a function of θ_{grid}.

Moreover, equations specifying energy loss at each specific switching transition remain useful when only a few switching transitions are subjected to hard switching as in the case of center-aligned modulation [11]. To illustrate losses in such scenarios, Fig.14(b) compares the $C_{\rm oss}$-based losses resulting from hard-switching transitions I and II ($P_{\text{Coss(trI+trII)}}$)) with the conduction losses ($P_{\text{conduction}}$) in the T-type bridge switches. Such hard-switching may occur due to insufficient tank current available for the ZVS of MOSFETs. These losses are plotted for the time-varying input voltages, v_{po} and v_{on}, shown in Fig. 14(c). The charge-equivalent capacitances of two types of SiC MOSFETs, as illustrated in Fig. 3, are utilized for the calculation. While $C_{\rm oss}$-based losses are relatively low compared to the T-type

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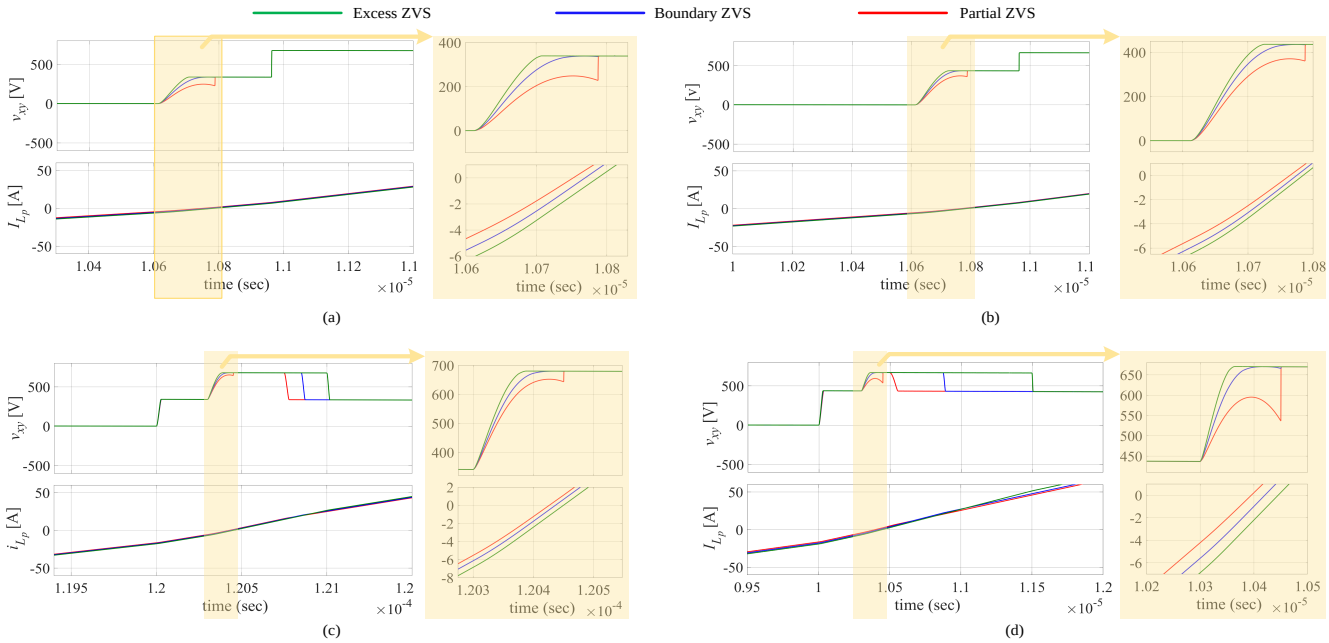

FIGURE 15. **Simulation results for verifying the calculation of the minimum ZVS current for (a) transition I at $\theta_{\text{grid}} = 30°$, (b) transition I at $\theta_{\text{grid}} = 40°$, (c) transition II at $\theta_{\text{grid}} = 30°$, and (d) transition II at $\theta_{\text{grid}} = 40°$.**

bridge conduction losses, they represent only the minimum possible losses, as they do not include hard-switching overlapping losses, which would further elevate overall switching losses. Therefore, it is important to accurately perform ZVS analysis for the T-type bridge, as provided in this work, to design the tank components and eliminate these switching losses entirely, thus enhancing the efficiency of the system.

VI. Simulation-Based Verification

To verify the accuracy of the ZVS analysis, simulations are performed using PLECS software for a T-type bridge-based dc-dc converter with a commutation sequence depicted in Fig. 4. The nonlinear output capacitances are introduced across the drain-to-source of an ideal MOSFET device in the simulation. The C_{oss} nonlinearity of the MOSFETs is modeled using a 1D look-up table, making C_{oss} a voltage-dependent quantity. The verification of minimum ZVS current is conducted at various dc input voltages corresponding to different grid angles throughout the grid cycle.

Simulation results validating the minimum ZVS current and time for transition I are presented in Figs. 15(a) and (b), while Figs. 15(c) and (d) show the simulation results for transition II. The verified simulation waveforms have been provided for two grid angles: 30° and 40°. To ensure the overall accuracy of the ZVS analysis, three distinct simulations are conducted at each of the specified grid angles by introducing a slight variation in the tank current, i_{L_p}. This variation is achieved by adjusting the duty ratios, d_p and d_n, of the T-type bridge, resulting in partial, boundary, and excess ZVS conditions. For instance, in Fig. 15(a), the minimum ZVS current for transition I at θ_{grid} = 30° is

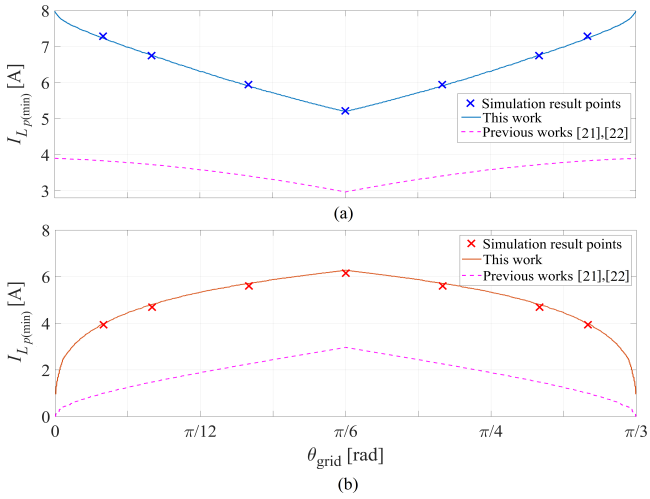

FIGURE 16. **Simulation-based verification of the minimum ZVS current at a range of grid angles for (a) transition I and (b) transition II, along with a comparison to prior studies [22]–[25].**

displayed. The three curves represent situations where the ZVS current exceeds (green), equals (blue), and falls below (red) the calculated ZVS current value.

Fig. 16(a) and Fig. 16(b) present simulation results obtained at a range of grid angles for transition I and transition II, respectively. These figures also illustrate the minimum ZVS current values obtained using the analysis provided in [22], [23], where the energies delivered or absorbed by the sources are excluded. Only the sum of the absolute values of charging and discharging energies required by the MOSFETs C_{oss} is considered in these previous works,

TABLE 4. Comparison of the calculated minimum ZVS current and ZVS time with simulation results and previous literature works.

Transition	θ_{grid}	Minimum ZVS current ($I_{L_{p(\min)}}$)			ZVS time (t_{zvs})	
		Simulation	Analysis	References [22]–[25]	Simulation	Analysis
I	30°	5.217 A	5.195 A	2.963 A	157.5 ns	167.8 ns
	40°	5.945 A	5.916 A	3.414 A	163.7 ns	175.9 ns
II	30°	6.154 A	6.217 A	2.963 A	136.8 ns	143.7 ns
	40°	5.602 A	5.643 A	2.256 A	120.7 ns	124.1 ns

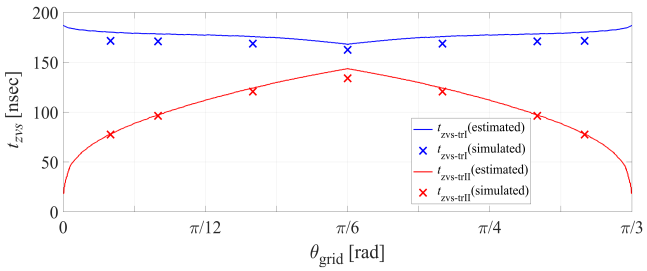

FIGURE 17. Simulation results for verifying the calculation of ZVS time during transition I and transition II at a range of grid angles.

potentially leading to percentage errors as high as 50%. The corresponding minimum ZVS current values, along with a comparison to previous literature, are further detailed in TABLE 4. Moreover, the estimated ZVS times are also verified through simulations, as illustrated in Fig. 17 and tabulated in TABLE 4.

VII. Experimental Verification

Experiments are conducted on a 20-kW ac-dc converter circuit comprising a grid-tied 3-ϕ Unfolder followed by a T-type primary bridge-based resonant dc-dc converter, as shown in Fig. 18. For a 480 V line-to-line (rms) 3-ϕ input voltage to the Unfolder circuit, both v_{po} and v_{on} vary from 0 V to 588 V. The half-bridge MOSFETs must withstand peak voltage stress equal to the peak of the line-to-line grid voltage, which is 678 V. Furthermore, the common-source MOSFETs must withstand peak voltage stress equal to the peak of either v_{po} or v_{on} voltage, which is 588 V. Additionally, MOSFETs are selected considering grid voltage fluctuations of $\pm$10%. The MOSFETs employed in the T-type bridge are specified in TABLE 5. The commutation pattern shown in Fig. 4 is applied to the T-type bridge. The T-type bridge output connects to the LCL-resonant tank circuit with a diode bridge rectifier on the secondary side.

The subsequent two subsections present the experimental results for verifying the calculations for ZVS requirements and validating the calculation of total C_{oss}-based switching losses, respectively.

A. Experimental verification of the ZVS requirements

To verify the ZVS analysis, the complete unfolding-based ac-dc conversion system is operated at its rated output power of 20 kW. The 3-ϕ grid input voltages of 480 V are emulated with the California Instruments MX-30 power supply. The output of the converter connects to the NH Research 9300 dc

TABLE 5. SiC MOSFETs used in the hardware setup.

Component	Description
Half-bridge MOSFETs (HB) S_{x1}, S_{x2}, S_{y1}, S_{y2}	Onsemi NVH4L020N120SC1 1200 V, 28 mΩ
Common-source MOSFETs (CS) S_{x3+}, S_{x3-}, S_{y3+}, S_{y3-}	Onsemi NVH4L040N120SC1 1200 V, 56 mΩ

power supply, which is utilized in a battery mode to emulate the load. The commutation sequence depicted in Fig. 4 is implemented with a staggering time of 200 ns between transition I and transition II. The tank circuit components are designed to ensure that the instantaneous current values of i_{L_P} during switching transitions are greater than the minimum ZVS currents required throughout the grid cycle. The values of tank circuit components are L_p = 29.3 μH, C_{pp} = 120.1 nF, and L_s = 6.23 μH. The LCL-resonant tank with an appropriate quality factor renders the tank current i_{L_P} fairly sinusoidal, as seen in Fig. 19. Therefore, the fundamental harmonic approximation is used to determine the instantaneous value of i_{L_p} during switching transitions and v_{Cpp} voltage variation throughout the grid cycle. Fig. 20 depicts the variation in voltage, v_{xy}, and current, i_{L_p}, throughout the grid cycle. As the two duty ratios, d_p and d_n, are varied to maintain sinusoidal grid currents, the instantaneous value of i_{L_p} available during transitions I and II also varies. This figure confirms the continuous ZVS operation of the T-type bridge throughout the grid cycle. To further validate ZVS conditions, transition II is analyzed at different grid angles, noting minimum ZVS currents and ZVS times. Fig. 21 displays three cases including a boundary ZVS case, an excess ZVS case, and two partial ZVS cases, each of which is explained in the following:

1) Boundary ZVS case

Fig. 21(a) illustrates an instant in the grid cycle when $\theta_{\text{grid}} = 35°$. The available tank current at the switching transition II, $I_{Lp(\text{tr})}$ of 6.3 A matches closely with the calculated minimum ZVS current, $I_{Lp(\min)}$ of 6.24 A. The boundary ZVS case is evident from the zero crossing of i_{L_p} coinciding with the drain-to-source voltage reaching zero.

2) Excess ZVS case

Fig. 21(b) shows an instant when $\theta_{\text{grid}} = 38°$. At this moment, the available current is much higher than the ZVS

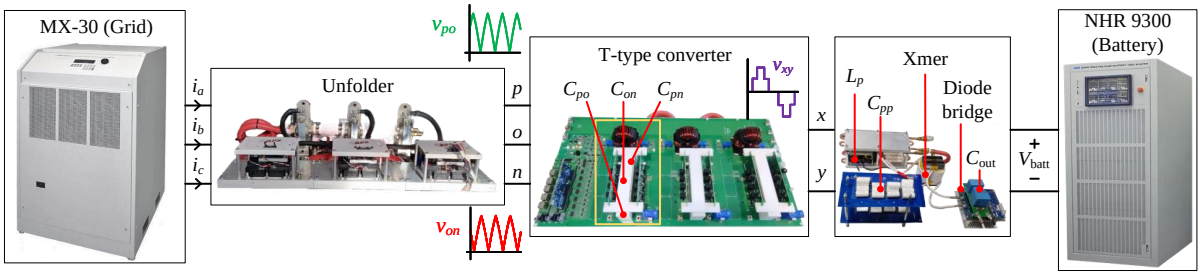

FIGURE 18. **A 20-kW hardware prototype of an unfolding-based ac-dc converter comprising a 3-ϕ Unfolder, the T-type primary bridge, and the LCL-resonant tank circuit, along with passive diode rectification.**

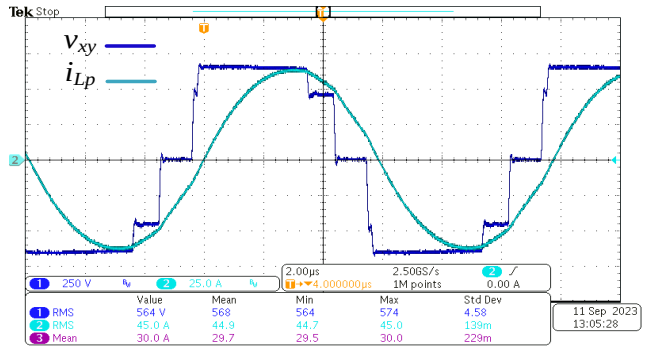

FIGURE 19. **Hardware results of the T-type bridge output voltage, v_{xy}, and tank current, i_{L_p}, at one instance of a grid cycle, with an output power of 20 kW.**

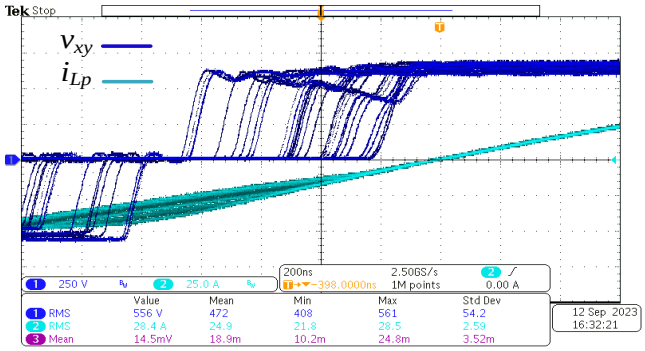

FIGURE 20. **Experimental results showing the variation of the v_{xy} and i_{L_p} throughout the grid cycle in Tektronix MDO3014 oscilloscope's infinite persistent mode. The leftmost leading edge of the v_{xy} waveform corresponds to transition I for $\theta_{\text{grid}} = 0^\circ$, where $v_{po} = v_{pn} = 588$ V and $v_{on} = 0$ V. The rightmost leading edge corresponds to $\theta_{\text{grid}} = 30^\circ$, where $v_{po} = v_{on} = v_{pn}/2 = 339$ V. A similar pattern is repeated in all other Unfolder sectors.**

current required for transition II, as evidenced by the zero crossing of the current lagging the time instant when the drain-to-source voltage falls to zero. The available tank current of 6.5 A is higher than the calculated minimum ZVS current of 6.2 A, $I_{Lp(\text{tr})} > I_{Lp(\text{min})}$, resulting in a complete ZVS with a higher current than required. The corresponding ZVS times are calculated using (29), as discussed earlier. Fig. 21(e) shows another excess ZVS case at $\theta_{\text{grid}} = 45^\circ$.

Furthermore, a special excess ZVS case is shown in Fig. 21(f), where $v_{po} = v_{on}$ at $\theta_{\text{grid}} = 30^\circ$. In this case, the staggering time is not required, as mentioned earlier. The corresponding minimum ZVS current can be calculated following the ZVS analysis described in this paper.

3) Partial ZVS case

To confirm the minimum ZVS current calculation more precisely, the load is gradually reduced from the full power of 20 kW, and the corresponding waveforms are observed. Fig. 21(c) shows the case when the load is slightly reduced and the current available at transition II, which is 5.7 A, is slightly less than the required current of 6.03 A, $I_{Lp(\text{tr})} < I_{Lp(\text{min})}$, resulting in partial ZVS. Partial ZVS can be observed as the drain-to-source voltage of switch S_{x1} is slightly higher than zero at the zero crossing point of the tank current i_{L_p}. This signifies the accuracy of the estimated ZVS current value. The load is further reduced to observe the partial ZVS condition more clearly and corresponding waveforms are shown in Fig. 21(d). In this case, the available current of 4.2 A is much lower than the calculated ZVS current value of 5.42 A at $\theta_{\text{grid}} = 46^\circ$. It is important to note that the minimum ZVS current values vary with grid angle. The calculated values for each of these instances are provided in TABLE 6, along with the experimental results.

TABLE 6 confirms the experimental validation of the ZVS analysis. The percentage errors between the estimated minimum ZVS currents and the corresponding experimental values are less than 1%. It can be further observed that, although calculations based on previous works consistently suggest that the minimum ZVS current requirement is always met for all six cases, the proposed analysis reveals that this postulation is not true. The proposed analysis validates partial, boundary, and excess ZVS conditions for all six cases.

Furthermore, the ZVS times for the boundary case and the excess ZVS case are measured from experimental data and compared with analytically calculated ZVS time values using (23) and (29) respectively. The comparative values, detailed in TABLE 6, indicate a maximum percentage error of 4.94%, affirming the close accuracy of the calculations.

With the analysis presented in this paper, ZVS-based soft-switching of the T-type bridge with a five-level output

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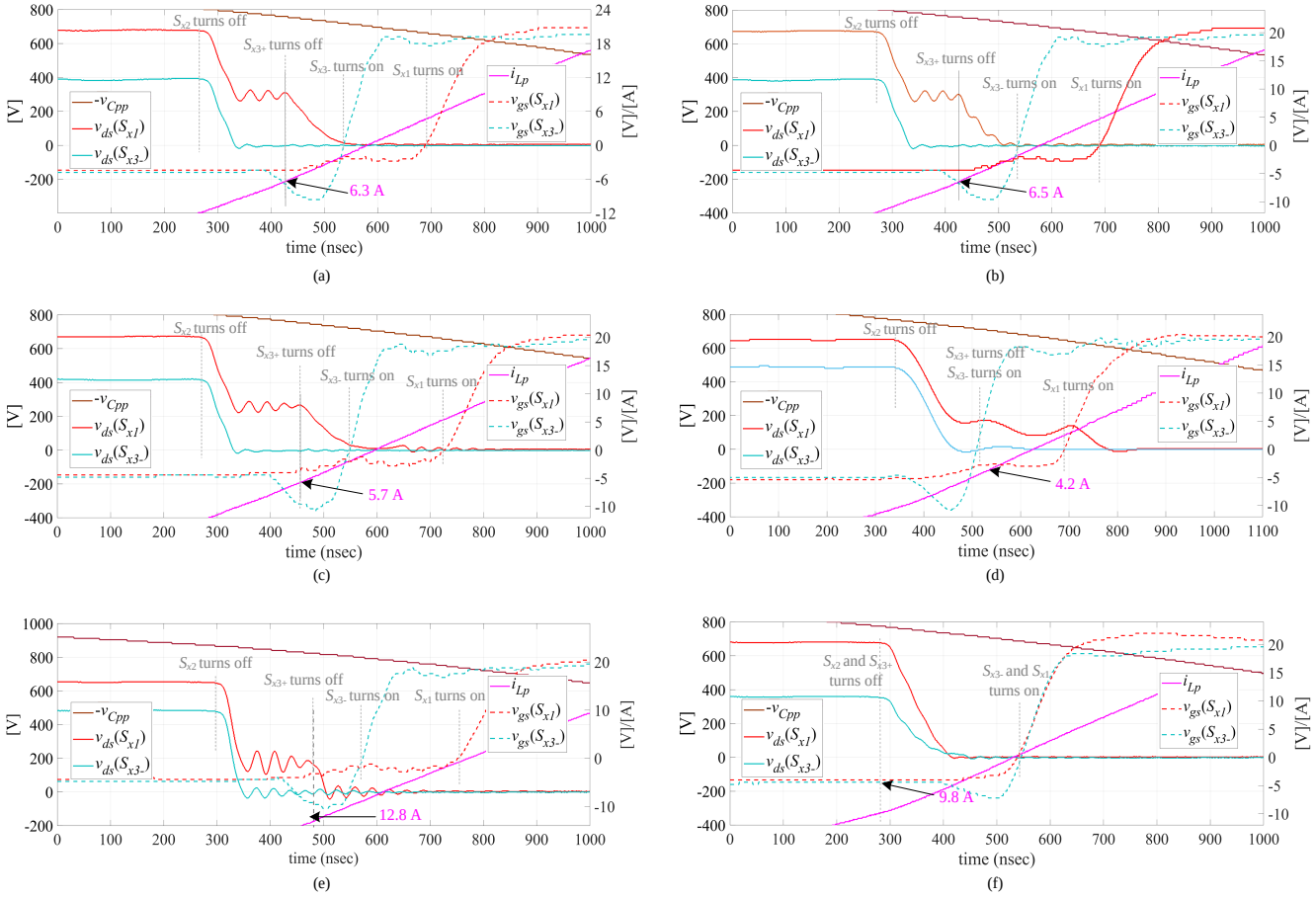


FIGURE 21. **Experimental results with a focus on the minimum ZVS current required for transition II during (a) boundary ZVS condition at $\theta_{\text{grid}} = 35°$, (b) excess ZVS case at $\theta_{\text{grid}} = 35°$, (c) partial ZVS case at $\theta_{\text{grid}} = 38°$, (d) partial ZVS case at $\theta_{\text{grid}} = 46°$, (e) excess ZVS case at $\theta_{\text{grid}} = 45°$, and (f) excess ZVS case at $\theta_{\text{grid}} = 30°$. The left *y*-axis shows drain-to-source voltages of switches S_{x1} and $S_{x3\text{-}}$, along with the reflected tank voltage, v_{Cpp}. The right *y*-axis shows gate-to-source voltages and the tank current, i_{L_p}.**

TABLE 6. **Comparison of calculated minimum ZVS current and ZVS time with hardware results and previous literature works.**

Figure	Case	Experimental $I_{Lp(\text{tr})}$	ZVS current ($I_{Lp(\text{min})}$)		ZVS time (t_{zvs})		
			Analysis	References [22]–[25]	Experimental	Analysis	% error
Fig. 21(a)	Boundary ZVS	6.3 A	6.2 A	2.6 A	137 ns	139.9 ns	2.1%
Fig. 21(b)	Excess ZVS	6.5 A	6.2 A	2.6 A	86 ns	90 ns	4.65%
Fig. 21(c)	Partial ZVS	5.7 A	6.03 A	2.4 A	-	-	-
Fig. 21(d)	Partial ZVS	4.2 A	5.4 A	1.8 A	-	-	-
Fig. 21(e)	Excess ZVS	12.8 A	5.5 A	1.9 A	24 ns	25 ns	4.16%
Fig. 21(f)	Excess ZVS	9.8 A	8 A	4.2 A	172 ns	180.5 ns	4.94%

voltage is successfully achieved throughout the grid cycle, as depicted earlier in Fig. 20. Also, the temperatures of the MOSFETs are maintained within safe limits with the maximum device temperature measured to be 62°C.

B. Experimental verification of total C_{oss}-based switching losses with open-circuited tank

To validate C_{oss}-based switching losses, the 3-ϕ Unfolder and tank circuit are disconnected and the T-type bridge is connected directly to two dc power supplies (Croma programmable dc power supply model 62024P-600-8). With the tank circuit disconnected, voltage-current overlapping switching losses do not occur. Also, the gate driver and control card are powered separately, avoiding the inclusion of their losses. The input capacitors (C_{po}, C_{on}, and C_{pn}) of the T-type bridge provide high-frequency switching currents, while the dc power supplies provide average power. The average input currents are measured using Agilent 34401A digital multimeters.

The losses are verified at different input voltages across the two input ports of the T-type bridge. The measured and estimated losses are shown in Fig. 22 as a function of the

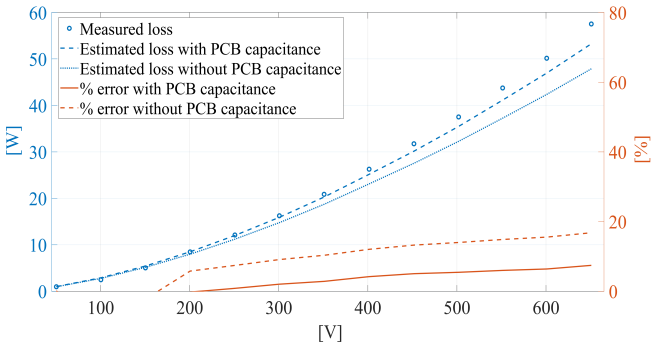


FIGURE 22. Experimental results of measured and estimated C_{oss}-based switching losses with an open-circuited tank are presented as a function of input voltage v_{pn} (where $v_{po} = v_{on} = v_{pn}/2$) at a switching frequency of 85 kHz. The results include losses with and without considering PCB capacitance (left *y*-axis), along with % error (right *y*-axis).

input voltage v_{pn}, where $v_{po} = v_{on} = v_{pn}/2$. The figure explores two scenarios: one incorporating losses attributed to printed circuit board (PCB) capacitances and another excluding these losses. Given the high power rating (20 kW) of the converter, the impact of PCB capacitances cannot be disregarded. To address this, PCB capacitances are measured between a switch node to an input node (*p* or *o* or *n*) of the T-type bridge, and a constant value of 150 pF is observed. The loss due to this lumped PCB capacitance is added in (30), reducing the error to less than 10%. Furthermore, precise methods such as calorimetric loss measurement can significantly minimize the percentage error in loss measurement by eliminating PCB trace resistances [26].

Another potential factor contributing to the slight difference between the measured and estimated C_{oss} losses, even with the inclusion of PCB capacitances, could be the hysteresis loss associated with C_{oss}. Recent studies suggest that up to 10% of the stored energy in SiC MOSFETs can be lost due to C_{oss} hysteresis loss, which is a phenomenon resulting in unequal charging and discharging energies of C_{oss}. The C_{oss} hysteresis losses vary for different semiconductor technologies, operating frequency, and dV/dt across the device. Super Junction MOSFETs exhibit highly unpredictable C_{oss} hysteresis losses, varying between manufacturers [34], while Gallium Nitride devices demonstrate an increase in losses with higher dV/dt across the device [35]. Incorporating this effect is complex [36], [37] and is beyond the scope of this paper. Nonetheless, the experimental results closely match the estimated values, which can aid in predicting C_{oss} losses in a T-type bridge for unfolding-based operation.

VIII. Conclusion

This work proposes an energy-based method to thoroughly analyze ZVS-based soft-switching in a T-type bridge within a single-stage unfolding-based ac-dc converter, which is applicable to any type of resonant tank circuit. The variations in the minimum ZVS current and ZVS time requirements throughout the grid cycle are shown, resulting from the time-varying input dc voltages and the nonlinear capacitance C_{oss}. Moreover, it is found that previous works determining ZVS currents for a T-type bridge result in underestimation, with a percentage error as high as 50%. This work also estimates the C_{oss} losses during each switching transition and provides a concise solution for total capacitive losses, enabling efficient comparison with other types of losses for overall design optimization.

Validation of the minimum ZVS current and time requirements is done with PLECS simulations by introducing nonlinear C_{oss} capacitances across the drain-to-source of the MOSFETs. The ZVS analysis is further verified using an unfolding-based ac-dc system with a T-type bridge-based dc-dc converter hardware prototype at an output power of 20 kW. It is found that the experimentally measured ZVS current requirements and ZVS times closely match the analytically calculated values with less than 1% and less than 5% percent errors, respectively. With the analysis presented in this paper, complete ZVS of the unfolding-based ac-dc conversion system is achieved throughout the grid cycle. Additionally, experiments conducted on an open-circuited T-type full-bridge validate the total C_{oss} losses over a switching cycle.

Appendix

A. Calculation for $C_{\text{eq,E}}$ and $C_{\text{eq,Q}}$

The MATLAB code is presented here for the calculation of the energy and charge equivalent capacitances.

```
Data = readtable('Coss_Vds_data.xlsx');
V_final = 1000;
Vds = Data{:,1};
Coss = Data{:,2};
arraylength = length(Vds);

for n = 1:arraylength-1
    dVds(n) = Vds(n+1)-Vds(n);
    mul_1(n) = dVds(n)*Coss(n);
    Coss_Vds(n) = Coss(n)*Vds(n);
    mul_2(n) = Coss_Vds(n)*dVds(n);
end
for i = 1:V_final
    for n = 1:arraylength-1
        if (Vds(n)<i)
           totalE(i) = mul_2(n)+totalE(i);
            totalQ(i) = mul_1(n)+totalQ(i);

       end
    end
    CeqE(i) = 2*totalE(i)/(i^2);
    CeqQ(i) = totalQ(i)/i;
end
```

Initially, the MOSFET datasheet is utilized to obtain C_{oss} - v_{ds} plot. The C_{oss} data points across var-

ious v_{ds} values are obtained from an online tool (eg. https://apps.automeris.io/wpd/) and stored in an Excel spreadsheet. It is observed that a logarithmic-logarithmic scale is most suitable for the computation of equivalent capacitances. The provided code enables the determination of $C_{\mathrm{eq,E}}$ and $C_{\mathrm{eq,Q}}$ at each data point as the voltage is incrementally varied from zero to the final specified voltage level.

REFERENCES

[1] S. S. G. Acharige, M. E. Haque, M. T. Arif, N. Hosseinzadeh, K. N. Hasan and A. M. T. Oo, "Review of Electric Vehicle Charging Technologies, Standards, Architectures, and Converter Configurations," in IEEE Access, vol. 11, pp. 41218-41255, 2023, doi: 10.1109/ACCESS.2023.3267164.

[2] H. Tu, H. Feng, S. Srdic and S. Lukic, "Extreme Fast Charging of Electric Vehicles: A Technology Overview," in IEEE Transactions on Transportation Electrification, vol. 5, no. 4, pp. 861-878, Dec. 2019, doi: 10.1109/TTE.2019.2958709.

[3] N. Xuan Bac, D. M. Vilathgamuwa and U. K. Madawala, "A SiC-Based Matrix Converter Topology for Inductive Power Transfer System," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4029-4038, Aug. 2014, doi: 10.1109/TPEL.2013.2291434.

[4] D. Das, N. Weise, K. Basu, R. Baranwal and N. Mohan, "A Bidirectional Soft-Switched DAB-Based Single-Stage Three-Phase AC–DC Converter for V2G Application," in IEEE Transactions on Transportation Electrification, vol. 5, no. 1, pp. 186-199, March 2019, doi: 10.1109/TTE.2018.2886455.

[5] H. L. Li, A. P. Hu and G. A. Covic, "A Direct AC–AC Converter for Inductive Power-Transfer Systems," in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 661-668, Feb. 2012, doi: 10.1109/TPEL.2011.2159397.

[6] W. W. Chen, R. Zane and L. Corradini, "Isolated Bidirectional Grid-Tied Three-Phase AC–DC Power Conversion Using Series-Resonant Converter Modules and a Three-Phase Unfolder," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9001-9012, Dec. 2017, doi: 10.1109/TPEL.2017.2652477.

[7] B. Zhang, S. Xie, X. Wang and J. Xu, "Modulation Method and Control Strategy for Full-Bridge-Based Swiss Rectifier to Achieve ZVS Operation and Suppress Low-Order Harmonics of Injected Current," in IEEE Transactions on Power Electronics, vol. 35, no. 6, pp. 6512-6522, June 2020, doi: 10.1109/TPEL.2019.2951795.

[8] A. Blinov, D. Zinchenko, J. Rąbkowski, G. Wrona and D. Vinnikov, "Quasi Single-Stage Three-Phase Filterless Converter for EV Charging Applications," in IEEE Open Journal of Power Electronics, vol. 3, pp. 51-60, 2022, doi: 10.1109/OJPEL.2021.3134460.

[9] S. Gurudiwan, R. Hatch, M. Mansour, H. Wang and R. Zane, "An 18 kW Battery Charger Module for Extreme Fast Charging Applications Using an Unfolding-Based AC-DC Topology," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1715-1722, doi: 10.1109/APEC43580.2023.10131542.

[10] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang and R. Zane, "3-Level Asymmetric Full-Bridge Soft-Switched PWM Converter for 3-Phase Unfolding Based Battery Charger Topology," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 2737-2743, doi: 10.1109/ECCE.2019.8913042.

[11] A. Zade et al., "A 21-kW Unfolding-Based Single-Stage AC–DC Converter for Wireless Charging Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 12, no. 1, pp. 8-27, Feb. 2024, doi: 10.1109/JESTPE.2023.3309588.

[12] C. R. Teeneti, R. Hatch, D. B. Yelaverthi, A. Kamineni, H. Wang and R. Zane, "Unfolder-Based Single-Stage AC-AC Conversion System for Wireless Charging Applications," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 5193-5198, doi: 10.1109/ECCE44975.2020.9235936.

[13] A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour and R. Zane, "Analysis and Mitigation of Sector Transition Distortions for Unfolding-based Grid-tied AC-DC Converters," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1945-1952, doi: 10.1109/APEC43580.2023.10131393.

[14] A. Zade, S. Gurudiwan, M. Mansour, B. Hesterman, D. Maksimović and R. Zane, "High-Bandwidth Control of a 21 kW Unfolding-Based AC-DC Converter Using Extra Element Theorem and Current Emulation Technique," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 698-705, doi: 10.1109/APEC48139.2024.10509068.

[15] M. S. Khan, S. S. Nag and A. Das, "A High Efficiency Non-Isolated Three-Phase Unfolding Based Electric Vehicle Powertrain," in IEEE Transactions on Industry Applications, doi: 10.1109/TIA.2024.3383803.

[16] D. Costinett, D. Maksimovic and R. Zane, "Circuit-Oriented Treatment of Nonlinear Capacitances in Switched-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 985-995, Feb. 2015, doi: 10.1109/TPEL.2014.2313611.

[17] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8063-8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.

[18] D. Costinett, D. Maksimovic and R. Zane, "Design and Control for High Efficiency in High Step-Down Dual Active Bridge Converters Operating at High Switching Frequency," in IEEE Transactions on Power Electronics, vol. 28, no. 8, pp. 3931-3940, Aug. 2013, doi: 10.1109/TPEL.2012.2228237.

[19] D. G. Bandeira, S. A. Mussa and I. Barbi, "A ZVS-PWM T-type isolated DC-DC converter," 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil, 2015, pp. 1-6, doi: 10.1109/COBEP.2015.7420107.

[20] D. G. Bandeira, T. B. Lazzarin and I. Barbi, "High Voltage Power Supply Using a T-Type Parallel Resonant DC–DC Converter," in IEEE Transactions on Industry Applications, vol. 54, no. 3, pp. 2459-2470, May-June 2018, doi: 10.1109/TIA.2018.2792446.

[21] S. Gurudiwan, A. Zade, R. Hatch, H. Wang and R. Zane, "ZVS Boundary Assessment for T-type-based Dual Active Bridge Series Resonant Converters using State-Plane Analysis," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 2098-2105, doi: 10.1109/APEC48139.2024.10509450.

[22] K. Kalayci, O. Demirel, U. Arifoglu and H. Hizarci, "Analysis of Three-Level T-Type LLC Resonant Isolated Bidirectional DC–DC Converter Under Three-Degrees-of-Freedom Modulation," in IEEE Access, vol. 11, pp. 60605-60625, 2023, doi: 10.1109/ACCESS.2023.3285265.

[23] D. Liu, Y. Wang, F. Deng, Q. Zhang and Z. Chen, "Zero-Voltage Switching Full-Bridge T-Type DC/DC Converter with Wide Input Voltage Range and Balanced Switch Currents," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10449-10466, Dec. 2018, doi: 10.1109/TPEL.2018.2800902.

[24] B. Zhang, S. Xie, Z. Li, P. Zhao and J. Xu, "An Optimized Single-Stage Isolated Swiss-Type AC/DC Converter Based on Single Full-Bridge With Midpoint-Clamper," in IEEE Transactions on Power Electronics, vol. 36, no. 10, pp. 11288-11297, Oct. 2021, doi: 10.1109/TPEL.2021.3073742.

[25] L. Jin, B. Liu and S. Duan, "ZVS Soft Switching Operation Range Analysis of Three-Level Dual-Active Bridge DC–DC Converter Under Phase Shift Control Strategy," in IEEE Transactions on Industry Applications, vol. 55, no. 2, pp. 1963-1972, March-April 2019, doi: 10.1109/TIA.2018.2872121.

[26] Cittanti, Davide, Cristoph Gammeter, Jonas Huber, Radu Bojoi, and Johann W. Kolar. 2022. "A Simplified Hard-Switching Loss Model for Fast-Switching Three-Level T-Type SiC Bridge-Legs" Electronics 11, no. 11: 1686. https://doi.org/10.3390/electronics11111686.

[27] G. Chindris, O. Pop, G. Alin and F. Hurgoi, "New PSPICE model for power MOSFET devices," 24th International Spring Seminar on Electronics Technology. Concurrent Engineering in Electronic Packaging. ISSE 2001. Conference Proceedings (Cat. No.01EX492), Calimanesti-Caciulata, Romania, 2001, pp. 158-162, doi: 10.1109/ISSE.2001.931039.

[28] U. Drofenik, A. Müsing and J. W. Kolar, "Voltage-dependent capacitors in power electronic multi-domain simulations," The 2010 International Power Electronics Conference - ECCE ASIA -, Sapporo, Japan, 2010, pp. 643-650, doi: 10.1109/IPEC.2010.5542316.

[29] Omsemi Silicon Carbide (SiC) MOSFET, NVH4L020N120SC1, N-Channel EliteSiC, 20 mohm, 1200 V, M1, TO247-4L, https://www.onsemi.com/download/data-sheet/pdf/nvh4l020n120sc1-d.pdf

[30] Omsemi Silicon Carbide (SiC) MOSFET, NVH4L040N120SC1, N-Channel EliteSiC, 40 mohm, 1200 V, M1, TO247-4L, https://www.onsemi.com/download/data-sheet/pdf/nvh4l040n120sc1-d.pdf

[31] K. Chen, Z. Zhao, L. Yuan, T. Lu and F. He, "The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC

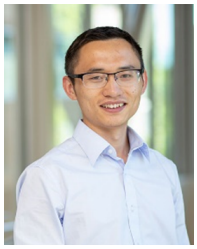
MOSFET," in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 333-338, Feb. 2015, doi: 10.1109/TED.2014.2362657.
[32] T. Funaki et al., "Characterization of SiC JFET for temperature-dependent device modeling," 2006 37th IEEE Power Electronics Specialists Conference, Jeju, Korea (South), 2006, pp. 1-6, doi: 10.1109/pesc.2006.1712168.
[33] P. Ralston et al., "High-Voltage capacitance measurement system for SiC power MOSFETs," 2009 IEEE Energy Conversion Congress and Exposition, San Jose, CA, USA, 2009, pp. 1472-1479, doi: 10.1109/ECCE.2009.5316221
[34] G. Zulauf, Z. Tong, J. D. Plummer and J. M. Rivas-Davila, "Active Power Device Selection in High- and Very-High-Frequency Power Converters," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6818-6833, July 2019, doi: 10.1109/TPEL.2018.2874420.
[35] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn and J. Rivas-Davila, "COSS Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10748-10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.
[36] Z. Tong, S. Park and J. Rivas-Davila, "Empirical Circuit Model for Output Capacitance Losses in Silicon Carbide Power Devices," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 998-1003, doi: 10.1109/APEC.2019.8721907.
[37] J. B. Fedison, M. Fornage, M. J. Harrison and D. R. Zimmanck, "Coss related energy loss in power MOSFETs used in zero-voltage-switched applications," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, USA, 2014, pp. 150-156, doi: 10.1109/APEC.2014.6803302.

Shubhangi Gurudiwan (Student Member, IEEE) completed her Bachelor's degree from Bhilai Institute of Technology, Durg, CG, India in 2016, and her Master's degree from the Indian Institute of Science, Bangalore, KA, India in 2018, both in Electrical Engineering. Since 2021, she has been pursuing her Ph.D. degree from the Electrical and Computer Engineering Department at Utah State University (USU) and ASPIRE NSF Engineering Research Center, Logan, UT, USA. Before joining USU, she worked as a Senior Research Engineer, and later as a Deputy Manager at Hind Rectifiers Ltd., Mumbai, MH, India. Her research interests include the design and control of dc-dc and ac-dc converters and the application of wide band gap devices and pulse width modulation techniques for EV charging systems.

She served as the chair of the USU IEEE-PELS student chapter in 2023. Additionally, she acted as a graduate student advisor for the USU team in the 2023 IEEE International Future Energy Challenge, which secured the third prize. She was a recipient of the 2024 Outstanding Graduate Research Assistant and Ph.D. Scholar of the Year Awards from the Department of Electrical and Computer Engineering, USU.

Aditya Zade (Student Member, IEEE) received his bachelor's (B.Tech.) degree from Sardar Patel College of Engineering, Mumbai, MH, India, in 2015, and the master's (M.Tech.) degree from the Indian Institute of Science, Bangalore, KA, India, in 2018, both in Electrical Engineering. Since 2021, he has been working toward a Ph.D. degree with the Power Electronics Department of Utah State University and ASPIRE NSF Engineering Research Center, Logan, UT, USA. He has worked as a Senior Research Engineer and Deputy Manager with Hind Rectifiers Limited, Mumbai, MH, India, from 2018 to 2021. His research interests lie primarily in the design, modeling, and control of power converters (ac-dc, dc-dc) as well as wireless power transfer, EV battery charging systems, and wide band-gap SiC/GaN-based converters.

He was the recipient of the gold medal during the course of his master's program and the IEEE Applied Power Electronics Conference and Exposition (APEC) 2024 best presentation award. Additionally, he served as a graduate student mentor to the undergraduate team from Utah State University, which won first place in the IEEE International Future Energy Challenge (IFEC) held in 2022.



Hongjie Wang (Senior Member, IEEE) received the B.S. degree from the University of Shanghai for Science and Technology, Shanghai, China, in 2009, the M.S. degree from Shanghai Jiaotong University, Shanghai, China, in 2012, and the Ph.D. degree from Utah State University, Logan, UT, USA, in 2018, all in Electrical Engineering.

From 2012 to 2014, he was a Senior Researcher with China Electric Power Research Institute, working on intelligent high-voltage equipment development and standardization. After graduating in 2018, he was a Postdoc Researcher at Utah State University for one year. Since 2019, he has been an Assistant Professor in the Electrical and Computer Engineering Department at Utah State University, where he also serves as the Co-Director of the Power Electronics Laboratory. He has co-authored more than 50 peer-reviewed publications and nine issued patents. His current research interests include dc power distribution, analysis, design, and control of resonant converters, extreme fast charging, grid interface power converters, health monitoring and diagnosis of power converters, second-life battery and battery management systems, and dynamic wireless power transfer for transportation electrification.

Dr. Wang was the recipient of the National Science Foundation Career Award in 2023. He was also the recipient of the 2022 Researcher of the Year Award and 2023 Outstanding Advisor of the Year Award from the Electrical and Computer Engineering Department at Utah State University, and the 2023 Undergraduate Research Mentor of the Year Award from the College of Engineering at Utah State University.

Regan Zane (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Colorado Boulder, Boulder, CO, USA, in 1999. He is currently the David G. and Diann L. Sant Endowed Professor with the Department of Electrical and Computer Engineering, Utah State University. He is the Director of the NSF Engineering Research Center for Advancing Sustainability through Powered Infrastructure for Roadway Electrification (ASPIRE).

Prior to joining Utah State University, he was an Assistant and Associate Professor with the University of Colorado Boulder with the Colorado Power Electronics Center and a Research Engineer with the GE Global Research Center, Niskayuna, NY, USA. He has co-authored more than 200 peer-reviewed publications and the textbook titled Digital Control of High-Frequency Switched-Mode Power Converters (New York, NY, USA: Wiley, 2015), and more than 30 issued patents. He has recent and ongoing research programs in power electronics for electric vehicle charging infrastructure, including extreme fast charging and static and dynamic wireless charging, battery management systems, dc microgrids, grid-tied and grid-interactive converters, and grid integration of energy storage and renewable energy.

Dr. Zane was the recipient of the National Science Foundation Career Award in 2004, the 2005 IEEE Microwave Best Paper Prize, the 2007 and 2009 IEEE Power Electronics Society Transactions Prize Letter Awards, and the 2008 IEEE Power Electronics Society Richard M. Bass Outstanding Young Power Electronics Engineer Award. He was also the recipient of the 2006 Inventor of the Year, the 2006 Provost Faculty Achievement, the 2008 John and Mercedes Peebles Innovation in Teaching, the 2011 Holland Teaching Awards from the University of Colorado, and the 2021 Researcher of the Year Award from Utah State University.