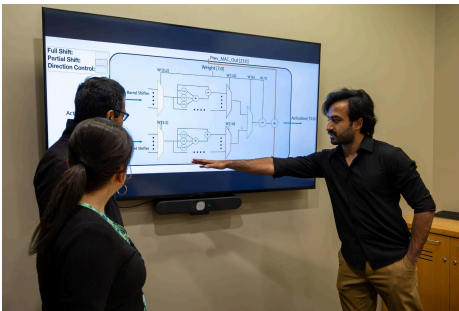


LogIQ and STRIVE: Innovative AI-Architecture to Increase Resilience, Reduce Power, and Improve Performance

08/06/2026



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Electrical & Computer Engineering

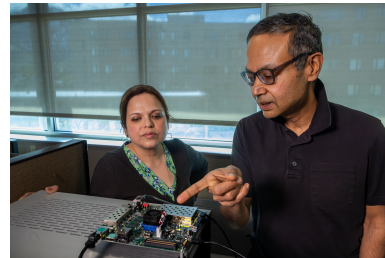
Abstract

AI-architecture must meet the demand for expanded operating boundaries, systems at the edge, and increase workloads through generative AI. Two technologies address several important problems contributing to these limits in AI hardware near and at the edge. The first, LogIQ, ensures a 2-3X reduction in area and power of the hardware accelerator with up to 8X improvement in performance compared to existing schemes for LLM operations. The second, STRIVE, makes AI-architecture at the edge more resilient to faults and increases throughput by parallel processing MAC units through decoupling dependencies.



LogIQ: A Novel Multiplier-free Systolic Array Hardware Accelerator for Large Language AI Models

Large language models (LLMs) have rapidly advanced state-of-the-art performance across domains, including question answering, summarization, code generation, and dialogue. As these models scale into billions of parameters and longer context windows, deploying them efficiently becomes increasingly difficult, especially in constrained environments like edge accelerators or low-power inference chips.



STRIVE: Empowering a Low Power Tensor Processing Unit with Fault Detection and Error Resilience

The error-resilient systolic array seeks to solve the challenges of fault-prone AI inference architectures at the edge. It achieves this through a low overhead detection technique for faulty Multiply-Accumulate (MAC) units in a systolic array AI hardware. This opens opportunities for device level process variation (PV) and fault tolerance at the circuit-architectural layer.

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Funding

This invention was made with government support, awarded by the NSF. The government has certain rights in the invention.

USU Reference Nos. C26013C25026