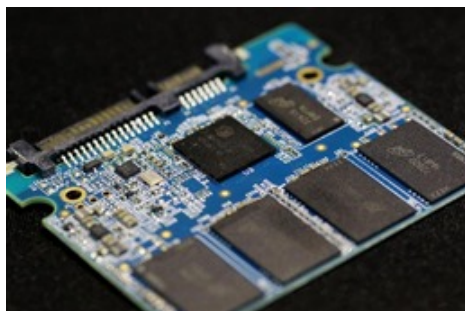


Low-Complexity Error Correction Algorithms for Data Communication and Storage Systems

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Electrical and Computer Engineering

Abstract

This patent describes a low-complexity error correction technique for digital communication systems. A decoder improves data reliability by adding a small random "perturbation" value to each reliability metric of an incoming data stream. Each reliability metric is calculated as a weighted combination of the raw channel signal and parity check results. When an error is detected, the decoder uses these adjusted reliability metrics to intelligently select and flip the least reliable bits until the error is resolved or a time limit is reached. This randomized approach helps the decoder avoid getting "stuck" on incorrect solutions, improving the odds of arriving at the correct data output, while using simpler, less resource-intensive hardware than traditional error correction methods.

What It Is

A randomized bit-flipping decoder for LDPC-style error correction that perturbs reliability metrics to guide bit-flip decisions during decoding.

Value Proposition

Reduces decoder hardware complexity and cost versus fully redundant error correction, while improving decoding accuracy by escaping local error-correction "dead ends."

Applicable Markets

Wired/wireless communications (e.g., Ethernet, 10GBASE-T), data storage systems, satellite/RF links, and any noisy digital channel needing efficient error correction.

Benefit

Traditional error correction often requires a tradeoff between accuracy and hardware cost: highly redundant coding schemes improve reliability but demand significant chip area, power, and processing overhead. This invention addresses that tradeoff by using randomized "noisy" perturbations to reliability metrics, a technique inspired by noisy gradient-descent bit-flipping algorithms. By nudging the decoder's confidence values with controlled randomness tied to the channel's noise characteristics, the system is statistically more likely to escape local error patterns and converge on the globally correct data output, rather than getting trapped by a plausible-but-wrong solution — a common failure mode in simpler bit-flipping decoders.

Because the entire process can be implemented with straightforward semiconductor gate logic (shift registers, counters, summers, and sign comparators) rather than complex iterative message-passing hardware, the design is well-suited to high-throughput, area- and power-constrained applications. The specification explicitly references potential use in standards like 10GBASE-T Ethernet, positioning this technology for markets including high-speed wired networking, wireless communications, optical/fiber links, and data storage — anywhere engineers need robust error correction without the die size or power budget for fully redundant coding schemes.

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Intellectual Property

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